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High Voltage Power Supply System and Front-End DAQ on FPGA/SoC for High Energy Particle Detectors

Settore scientifico-disciplinare: ING-INF/01 Electronics

DOTTORANDO: **Luis Guillermo García Ordóñez**

COORDINATORE: **Prof. Alberto Tessarolo**

SUPERVISORE DI TESI: **Prof. Sergio Carrato**

CO-SUPERVISORE DI TESI: **Dr. Maria Liz Crespo**

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Abstract

High energy physics experiments are based on complex detectors built with novel techniques frequently configured in multichannel arrays. These complex detectors create the need for custom-made related instrumentation and methods not found in commercial devices. The research activity presented in this thesis aims at developing a distributed High Voltage Power Supply System (HVPSS) network for hybrid Micro-pattern Gaseous Detectors (MPGD) similar to the ones used in the RICH-1 detector of the COMPASS experiment at CERN. The hardware design was tested in several conditions, including test beams at CERN in the SPS H4 beam line and with nuclear sources in the RD51 laboratory.

The HVPSS can polarize a hybrid-MPGD supplying up to 4 kV of bias voltage with 68 mV step precision. The system provides voltage and current monitoring of 15 mV and 3.9 pA, respectively, and HV compensation based on temperature and atmospheric pressure. Fast transient events can be detected with 2 ns timestamp resolution. The HVPSS is comprised of multiple channels galvanically isolated to provide a cascade interconnection topology. The communication is done trough a high voltage isolated network interface designed to decouple up to 2 kV between consecutive channels. A modified precise-time protocol was implemented for time synchronization using the network interface achieving 20 ns of time accuracy.

The modular architecture, as well as the reconfigurable capacity of the SoC-FPGA, opened the possibility of using the HVPSS as an instrument for other experiments. With few modifications, the developed system was successfully tested as a front-end Data Acquisition (DAQ) system for Water Cherenkov Detectors (WCD) in the context of indirect measurements of cosmic rays.

Each pulse captured with the DAQ was sampled and timestamped with 2 ns resolution. Pulse-shape discrimination algorithms were implemented for online particle classification. A

FIR-based correlation technique was used to classify three types of particles obtaining an overall accuracy of 84.3% with a latency of 224 ns.

This thesis first describes the basic physics concepts underneath these high energy particle detectors and their electronics. It is followed by the most relevant aspects of the design process for the HVPSS and its modifications leading to the DAQ for WCDs.

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Acronyms

μP Microprocessor.

ADC Analog to Digital Converter.

ASIC Application Specific Integrated Circuit.

COMBLOCK Comunication Block.

COMPASS Common Muon and Proton Apparatus for Structure and Spectroscopy.

DAC Digital to Analog Converter.

DAQ Data Acquisition System.

EDA Electronic Design Automation.

FIR Finite Impulse Response.

FMC FPGA Mezzanine Connector.

FPGA Field Programmable Gate Array.

GEM Gas Electron Multiplier.

GRB Gamma Ray Burst.

HEPD High Energy Particle Detector.

HV High Voltage.

HVIBNI High Voltage Isolated Bidirectional Network Interface.

HVPSS High Voltage Power Supply System.

IIC Inter-Integrated Circuit.

ILA Integrated Logic Analyzer.

JTAG Joint Test Action Group.

MCA Multichannel Analyzer.

MM Micro-Megas.

MPGD Micro-Pattern Gaseoud Detector.

MSGC Micro-Strip Gas Chamber.

MWPC Multi-Wire Proportional Chamber.

OSFA Open Source Framework Architecture.

PCB Printed Circuit Board.

PMT Photomultiplier Tube.

PPS Pulse-Per-Second.

PSD Pulse Shape Discrimination.

PTP Precise-Time-Protocol.

RICH Ring Imaging Cherenkov Counter.

RTL Register Transfer Level.

SoC System On Chip.

SPI Serial Peripheral Interface.

SPS Super Proton Synchrotron.

THGEM THick Gas Electron Multiplier.

TPC Time Projection Chamber.

UART Universal Asynchronous Receiver-Transmitter.

WCD Water Cherenkov Detector.

Introduction

Research in modern high energy physics depends heavily on the ability to extract information from the particles under study. Several techniques and detectors have been developed and improved over time. Recent advances in electronics, semiconductors, Field Programmable Gate Array (FPGA) and System on Chip (SoC) technologies, signal processing, and pattern recognition techniques, to mention a few, allow the development of state of the art instrumentation. New readout solutions offer the possibility to extract more information from the detector signals and at faster rates. Different types of detectors are combined in hybrid configurations to enhance their characteristics, increasing at the same time the complexity of the design of the associated electronics. This synergy between the development of new detectors and new electronics leads us to this thesis.

The main focus of this work is the research and development of a multichannel High Voltage Power Supply System (HVPSS) based on SoC-FPGA, used to polarize the electrodes of a hybrid micropattern gaseous detector (MPGD) similar to the ones used on the 83000-channel RICH-1 detector of the COMPASS experiment at CERN. The detector consists of two THick Gas Electron Multipliers (THGEMs) and one MicroMegas (MMs). The HVPSS was built to meet special requirements of high-resolution diagnostic, featuring automatic dynamic voltage control not available in commercial systems. This research work has been carried out as part of a collaboration between the Multidisciplinary Laboratory of the Abdus Salam International Centre for Theoretical Physics (MLAB-ICTP) and the COMPASS Group of the Italian National Institute of Nuclear Energy, Trieste Section (INFN-TS).

Specifically, the HVPSS requires to provide accurate current measurements, true real-time monitoring of the voltage and current to study the precise evolution of breakdown events, precise high voltage (HV) supply to polarize the electrodes of the detector, as well as to perform user-defined actions for pre-breakdown conditions and high-resolution time stamping to study the evolution of fast electrical transients. The system also needs to be modular and scalable with nanosecond synchronization among channels in different HV power domains.

Each HVPSS channel is based on a fully programmable System on Chip based on FPGA with an embedded microprocessor (SoC-FPGA) that provides HV control from 0 to -4 kV with 20 mV step resolution, with automatic compensation based on temperature and pressure measurements needed for stable operation of the detector. The system provides real-time current measurement at HV with 5 pA of amplitude resolution and 2 ns of time resolution to study fast transient phenomena. A High Voltage Isolation Bidirectional Network Interface (HVIBNI) is implemented for galvanic isolation in the communication among the different HVPSS channels. Each channel is ready to be connected in a HV power domain, and the communication with its neighbor channels is galvanically decoupled up to 2 kV_{rms} in continuous operating mode and 8 kV_{peak} for 16 minutes. In this network, a custom precise time protocol (PTP) provides time synchronization within 20 ns to study the propagation of fast transient phenomena through different channels.

During the Ph.D. program, a full-stack development of the different components of the HVPSS was carried out, including: the design and production of different printed circuit boards (PCB) comprising the modules of a HVPSS channel, the firmware, and control software of the FPGA and embedded microprocessor of the SoC, and the remote control software and GUI to interact with a PC. During the first stages of development, a single channel prototype was built and tested in one of the electrodes of a hybrid MPGD prototype (minipad) during a test beam in the SPS H4 beam line at CERN.

After the results of the first test, several upgrades were incorporated into the design leading to the second version of the HVPSS channel. Furthermore, seven channels were produced and tested in the RD51 laboratory at CERN. The minipad detector was taken into operation conditions by the HVPSS, and the performance of the system was tested by stimulating the detector with a nuclear source. Several communication tests among channels were conducted, including the performance of the high voltage isolated network interface and time synchronization among channels using PTP.

Several innovative tools were developed to achieve the goals presented in this thesis. The selection of a SoC-FPGA allowed the implementation of an open-source firmware architecture that provides a pre-built framework for the system developer to implement time-critical tasks on the FPGA and non-critical tasks, such as slow-control, in the microprocessor. The modular architecture provides common communication services between the FPGA, the microprocessor, and the PC simplifying the design process and granting system portability. The FPGA controls a high-speed 500 MHz Analog to Digital Converter (ADC) to capture fast-transient events with 2 ns resolution; while applying oversampling and decimation algorithms to increase the signal-to-noise ratio of the current measured by a picoammeter board. These simultaneous high-speed event acquisition and low-speed high-resolution measurement in the same channel are not common in commercial HV power suppliers.

The amplification gain of a hybrid MPGD depends on the voltage difference between consecutive electrodes. This means that each voltage channel is referred as a previous voltage level instead of the absolute ground. There are two configuration methods for polarizing the MPGD. The first method sets all the power supplies to a common reference and controls dynamically all the voltages between electrodes. The second method referred to the local ground of each power supply to the previous electrode in cascade mode controlling locally every variation of the HV. The HVPSS is designed to support both configurations that can be used depending on the specific needs of the detector.

The HVIBNI allows to freely expand the number of HV channels with galvanic decoupling. This feature is a strong advantage when compared with similar commercial and custom power supply systems. The HVIBNI provides four bidirectional HV decoupled lines with a maximum transmission frequency of 100 MHz, providing a privileged communication network among channels.

Another remarkable advantage of the HVPSS over similar systems is the time synchronization among channels. A PTP variation is executed continuously in the FPGA using the HVIBNI to synchronize the clocks of all the channels achieving time synchronization within 20 ns. This is comparable with the 100 ns requirements of the IEEE 1588-2008 standard for a PTP grandmaster with the added benefit of the HV decoupling.

The modular hardware/software architecture of the HVPSS allowed being reconfigured as a Data Acquisition System (DAQ) for Water Cherenkov Detectors (WCD) in the context of indirect detection of cosmic rays. This DAQ-WCD is a repurposed HVPSS channel with few modifications. The system was tested in an experimental WCD base station in the School of

Physics and Mathematics Sciences of San Carlos University in Guatemala (ECFM-USAC). The aim of this research is to provide an instrument to detect and study high energy astronomical sources by indirect measurements of Extensive Air Showers (EAS). Experimental data were collected by the DAQ-WCD over several weeks, and based on the data analysis novel pulse-shape discrimination algorithms for online classification of cosmic rays signals have been developed and implemented in the FPGA.

Objectives of the Thesis

The objectives of this thesis can be summarised as follows:

1. To design a HV power supply system that meets the requirements for a hybrid-MPGDs.
    (a) To design the different hardware modules that comprise each channel of the HVPSS.
    (b) To produce several channels to polarize the different electrodes of the MPGD.
    (c) To develop a HV isolated network to communicate among channels.
    (d) To test the system on a MPGD under beam conditions and with radioactive sources at CERN.
2. To develop and implement the firmware and control software required to operate the HVPSS.
    (a) To implement on the FPGA different RTL blocks for time-critical tasks.
    (b) To develop a microprocessor firmware to provide communication and user-specific tasks to interface with the control system.
    (c) To implement communication protocols for time synchronization among the HVPSS channels.
    (d) To design a control system with a graphical user interface for remote control from a PC.
3. To implement the HVPSS as a data acquisition system for indirect measurements of cosmic rays on water Cherenkov detectors.
    (a) To develop an algorithm for online pulse shape discrimination on the FPGA.

Scientific Publications

During this research, a total of fourteen publications in journals and conferences have been produced, broken down into the following topics: seven publications related to the HVPSS for MPGD, three publications in the context of front-end DAQ for WCD, and four related to other topics.

In the context of HVPSS for MPGDs:

[1] K. S. Mannatunga et al., “Design for Portability of Reconfigurable Virtual Instrumentation,” Apr. 2019. doi: 10.1109/spl.2019.8714446.

[2] R. A. Melo, B. Valinoti, M. Baly Amador, L. G. Garcia, A. Cicuttin, and M. Liz Crespo, “Study of the Data Exchange between Programmable Logic and Processor System of Zynq-7000 Devices,” 2019 10th South. Conf. Program. Log. SPL 2019 - Proc., pp. 3–8, 2019.

[3] J. Agarwala et al., “MPGD-based photon detectors for the upgrade of COMPASS RICH-1 and beyond,” J. Instrum., vol. 15, no. 9, 2020.

[4] S. Carrato et al., “A scalable High Voltage Power Supply System with system on chip control for Micro Pattern Gaseous Detectors,” Nucl. Instrum. Methods Phys. Res. Sect. Accel. Spectrometers Detect. Assoc. Equip., vol. 963, p. 163763, May 2020, doi: 10.1016/j.nima.2020.163763.

[5] L. G. García et al., “High Voltage Isolated Bidirectional Network Interface for SoC-FPGA Based Devices,” in Lecture Notes in Electrical Engineering, Springer International Publishing, 2021, pp. 280–285. doi: 10.1007/978-3-030-66729-0_34.

[6] W. Florian et al., “An Open-Source Hardware/Software Architecture for Remote Control of SoC-FPGA Based Systems,” in Lecture Notes in Electrical Engineering, Springer International Publishing, 2022, pp. 69–75. doi: 10.1007/978-3-030-95498-7_10.

[7] L. G. G. Ordóñez et al., “Multichannel Time Synchronization Based on PTP through a High Voltage Isolation Buffer Network Interface for Thick-GEM Detectors,” Instruments, vol. 6, no. 1, p. 11, Feb. 2022, doi: 10.3390/instruments6010011.

In the context of DAQ for WCD:

[1] L. G. G. Ordóñez et al., “DAQ platform based on SoC-FPGA for high resolution time stamping in cosmic ray detection,” Jul. 2019. doi: 10.22323/1.358.0266.

[2] L. G. Garcia et al., “Muon–Electron Pulse Shape Discrimination for Water Cherenkov Detectors Based on FPGA/SoC,” Electronics, vol. 10, no. 3, p. 224, Jan. 2021, doi: 10.3390/electronics10030224.

[3] L. G. G. Ordóñez et al., “Pulse Shape Discrimination for Online Data Acquisition in Water Cherenkov Detectors Based on FPGA/SoC,” Jul. 2021. doi: 10.22323/1.395.0274.

Other contributions:

[1] A. Cicuttin, L. D. Micco, M. L. Crespo, M. Antonelli, L. Garcia, and W. Florian, “Physical implementation of asynchronous cellular automata networks: mathematical models and preliminary experimental results,” Nonlinear Dyn., Jul. 2021, doi: 10.1007/s11071-021-06754-z.

[2] M. L. Crespo et al., “Remote Laboratory for E-Learning of Systems on Chip and Their Applications to Nuclear and Scientific Instrumentation,” Electronics, vol. 10, no. 18, p. 2191, Sep. 2021, doi: 10.3390/electronics10182191.

[3] G. D. Alexeev et al., “Probing transversity by measuring λ polarisation in SIDIS,” Phys. Lett. Sect. B Nucl. Elem. Part. High-Energy Phys., vol. 824, 2022.

[4] R. S. Molina et al., “Compression of NN-Based Pulse-Shape Discriminators in Front-End Electronics for Particle Detection,” in Lecture Notes in Electrical Engineering, Springer International Publishing, 2022, pp. 93–99. doi: 10.1007/978-3-030-95498-7_13.

Thesis Outline

This thesis is structured as follows. Chapter 1 presents the basic concepts of high energy particle detectors and their working principle. Chapter 2 describes the hybrid MPGD and the requirements of the HVPSS in the context of the COMPASS experiment and its RICH-1 detector. Chapter 3 presents the hardware selection and design process of the different printed circuit boards comprising a HVPSS channel. Chapter 4 describes the firmware design of the FPGA and the embedded microprocessor, including the architecture of the system and the communication between the Register Transfer Level (RTL) blocks on the FPGA and the microprocessor. Chapter 5 describes the concepts behind indirect cosmic rays studies and the experimental ground station used for the development of the front-end DAQ for WCD. This chapter also describes the system modifications at hardware and firmware level finalizing with the description of the concepts of pulse-shape discrimination used for particle classification. Chapter 6 presents the results of the experiments carried out during the research program related to the HVPSS for MPGDs and the DAQ for WCD. Finally, the conclusions and final remarks are presented in Chapter 7.

Chapter 1

High Energy Particle Detectors Electronics

The first Scientific Committee of the Italian National Institute of Nuclear Energy (INFN), CSN1, deals with experiments to broaden our knowledge in sub-nuclear physics, exploring the frontiers up to the instrument limitations [1]. Eighteen experiments are followed by the Committee and are located in several national and international laboratories. The nuclear and sub-nuclear reactions studied cover a vast interval of the center of mass energies, from sub-eV up to TeV at high energy colliders. Consequently, each experiment developed specific and challenging solutions for its particle identification requirements, adapting the techniques to the interval of energies to be covered, from eV particles produced in low-energy machines up to GeV ones produced at colliders [2].

The modern development of High Energy Particle Detectors (HEPD) applies a wide range of methods and technologies for particle identification. Before developing custom electronics that meet the specific requirements of a detector, it is essential to understand the relevant physics concepts and principles that make it work. This chapter explains the basics of the working principles of common HEPDs and the physics behind them.

1.1 Electronic Components of HEPD

Independently of their working principle, HEPDs are used for three basic functions: detecting the track of a particle (some including position sensing), measuring its energy, and recording its arrival time. The control electronics surrounding the detectors should, at the same time, correspond to each of these functions as follows.

- To detect the presence of a particle:
  - Readout system for small signals, including analog-to-digital converters with enough sampling frequency and amplitude resolution to acquire the detector signals.
- To measure the energy spectrum:
  - Digital pulse processing and feature extraction of the digitized signals.
- To record relative timing between events:
  - High-resolution timing measurements.
- To communicate with other detectors:
  - Network interface to communicate among detectors channels in a scalable architecture.
- Slow control and polarization electronics (e.g., HV power supplies).

Novel detection techniques are often not based on new inventions but on combining existing technologies. For every development of a new detector, the control electronics usually undergo an *ad-hoc* design process to meet its requirements. As the complexity of the detectors increases, several challenges make the design of the electronic system more complex. Baseline fluctuations depending on environmental variables (e.g., temperature and pressure), noise over the signal and timing measurements, clock synchronization among channels, and random fluctuations in the detector's outputs are some of the frequent issues in most HEPDs [3].

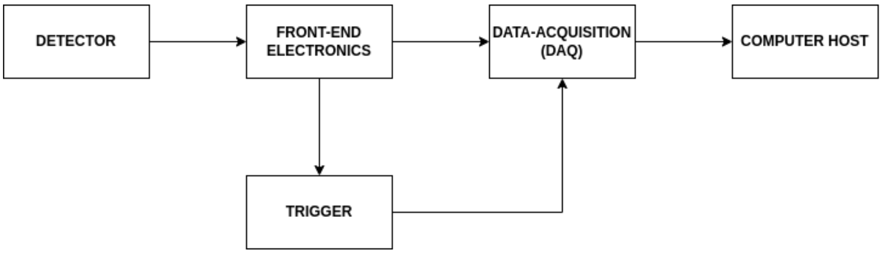


Figure 1.1: Typical simplified architecture of HEPD experiments.

Fig. 1.1 represents the typical architecture of high-energy experiments. Every block, excluding the detector, involves specific electronics, hardware, and software. The electronics aim to acquire only interesting data and suppress useless data and noise. Due to the evolution of technology, particularly in ADCs and FPGAs devices, new architectures in experimental physics have been proposed. These are based on fully digital signal processing, as shown in Fig. 1.2. In experiments of the new generation, the trend is to digitize the detector output, then digitally process this signal to obtain the trigger, finalizing with the data transfer to a host computer [4].

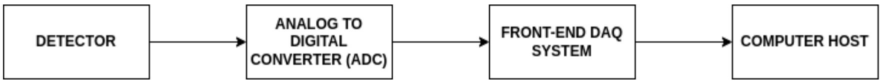


Figure 1.2: Typical new generation architecture of experiments.

The front-end electronics and the data acquisition system are merged in this new architecture. The readout of events and the control of the front-end electronics are carried out by modern FPGAs and SoC-FPGA devices or application specific integrated circuits (ASICs).

The traditional trigger systems provide only limited possibilities of triggering methods. The LHCb experiment has proposed upgrading its current readout architecture by removing the first-level hardware trigger. The new readout system will record every event and send data to a trigger selection process performed entirely by software running in a computing farm [5]. A free-running DAQ is under development for the AMBER experiment at CERN, including FPGA modules and advanced software processing to work in triggerless mode [6].

This thesis focuses on a front-end DAQ electronic system for MPGDs and WCD based on the requirements of modern HEPDs. The following sections describe the basics of the physics, the most common types of detectors, and the state of the art of readout electronics for HEPDs. The specifics of the MPGDs and WCDs are described in Chapters 2 and 5 respectively.

1.2 Interaction of Particles With Matter

Before developing any electronics to study high energy particles, it is essential to understand how to detect them. If one particle travels in any material, it has a probability of interacting with the atoms composing that material. The primary interaction is electromagnetic for charged particles (e.g., electrons, muons). If the charged particle has enough mass (proton, alpha particles, charged hadrons), it can also undergo a nuclear interaction. In these interactions, an energy exchange happens between the atoms of the material and the particle. The charged particle interacts with the electromagnetic fields of the electrons, and the nuclei of the material produce elastic collisions with these objects [7]. Electromagnetic interactions are responsible for particle scattering, ionization and excitation of atoms, bremsstrahlung transition, and Cherenkov radiation. Ionization and bremsstrahlung change the particle trajectory due to interaction with the nuclei [8]; in contrast with Cherenkov and transition radiation that have negligible energy loss and do not change the direction of the particle motion.

1.2.1 Cherenkov Effect and Light Collection

When a charged particle moves in a transparent medium with a velocity v exceeding the velocity of light c/n in that medium (where n is the refractive index), it emits a specific type of radiation called Cherenkov radiation. The following expression can describe this effect:

$$\cos\theta_c = \frac{1}{n\beta} \tag{1.1}$$

In this equation $\beta = v/c$. The radiation is emitted in a cone with angle θ_c in a phenomenon similar to a mechanical shockwave produced from a plane breaking the speed of sound (Fig. 1.3). Cherenkov radiation is widely used for charged particle identification since θ_c depends on the particle velocity. The number of Cherenkov photons emitted in the optical wavelength range of 400-700 nm per unit of length can be estimated as:

$$\frac{dN}{dx} = 490\sin^2\theta_c[cm-1] \tag{1.2}$$

The working principle of several detectors depends on the detection of these photons, either by observing their trajectory and calculating their angle or by counting the number of photons emitted.

1.2.2 Photoelectric Effect

Gamma rays can interact with matter in many different ways. One of the most important interactions is the photoelectric effect. In these processes, a photon is completely absorbed in

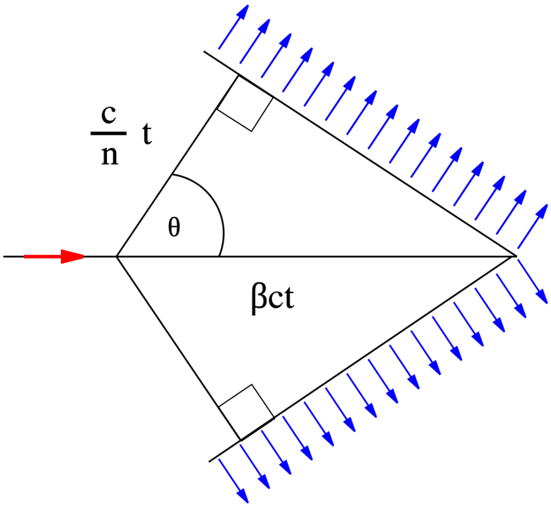


Figure 1.3: Cherenkov radiation emission angle shown for the ideal case of no dispersion.

the interaction with an atom. The electron can be excited to a higher level within the atom or set free (called photoelectron) if the energy transferred is sufficient. This effect happens when the energy of the photon $E = hv$ (where h is Plank's constant and v is the photon's frequency) is higher than the energy to keep an electron in one of the atom's orbitals called binding energy E_B. The electron's kinetic energy is the result of the difference between both energies.

$$K_e = hv - E_B \tag{1.3}$$

In addition to a photoelectron, the interaction also creates a vacancy in one of the energy levels. Atomic electrons are rearranged, and characteristics X-rays are emitted. Sometimes an electron from the outer shell falls into the vacant orbital with enough energy to expel another electron. This product is known as Auger electron instead of X-rays. The cross-section of the gamma rays to produce a photoelectron depends on the atomic number Z and the energy E_γ of the gamma rays.

1.3 Types of Detectors

Three main methods for detecting charged subatomic particles are detection based on gas ionization, detection based on semiconductors, and scintillation.

1.3.1 Gaseous Detectors

The basic principle of detection in gas starts with the inelastic collisions between the incident particle and gas molecules. These collisions lead to excitation of the medium, followed by emission of light and ionization. The primary electrons (electrons produced by ionization) can often have enough energy to ionize the medium further. The number of electron-ion pairs produced usually is a few times larger than the number of primaries. Under the influence of an applied electric field, electrons and ions drift in opposite directions towards the electrodes. The drift velocity and diffusion of electrons depend very strongly on the gas's specific characteristics. Nobel gases are a mixture of poly-atomic gases to achieve large drift velocities. The electron component is faster than the ions, which determines the detected signal's characteristic shape: a fast rise followed by a gradual increase. The slow component limits the time resolution of the counter, is called the ion tail, and is usually removed by differentiation. In uniform fields, the number of initial electrons N_0 multiply over a length x, forming an electron avalanche of size $N = N_0 e^{\alpha x}$ where α is a parameter that depends on the gas. Gas amplification (N/N_0) of 10^3 - 10^4 is needed to provide signals with sufficient amplitudes for conventional electronics. Several types of detectors increase this gain by using different techniques to multiply the number of electrons generating additional cascades in multiple stages of avalanche multiplication.

In 1908 the first wire counter was used by Rutherford in the study of natural radioactivity. After that, the advances and breakthroughs in instrumentation lead to the development of new technologies. In 1968 the Multi-Wire Proportional Chamber (MWPC) was developed with a fully parallel readout for an extensive array of sensing elements giving Georges Charpak a Nobel Prize in Physics in 1992. This invention revolutionized particle detection, which moved from optical-readout devices (cloud chamber, emulsion, or bubble chambers) to the electronics era. MWPC is a relatively simple and robust detector. It is most useful when charged particle tracks must be detected and localized over a large area. The increasing demands of particle physics experiments have led to the improvement of MWPCs over the years. Advanced detectors have been developed, such as Drift chambers (1971), Time Projection Chambers (TPC) in 1978, Ring-Imaging Cherenkov Counter (RICH) (1977), and Resistive Plate Chambers (1981). The advances in microelectronics and printed circuit technology favored the invention of novel micro-structured gas-amplification devices. In 1988 the Micro-Strip Gas Chamber (MSGC) achieved position resolution of a few tens of microns and particle fluxes exceeding MHz/mm^2. Two fundamental weakness of the MSGC was the formation of deposits on the electrodes affecting the gain, the susceptibility to spark-induced damages in the presence of highly ionizing particles could not be resolved. The detailed studies of their properties led to the development of a family of alternative structures called Micro-Pattern Gaseous Detectors (MPGD) (1999) [9]. By 2008, the interest in the development of MPGDs led to the establishment of RD51 collaboration at CERN [10]. Many technologies became available and affordable, new detection concepts are still being introduced, and existing ones are substantially improved by developing hybrid detectors [11], or diamond-like carbon resistive electrodes [12].

1.3.2 Scintillator Detectors and Cherenkov Detectors

Scintillators depend on producing charged particles within a medium to generate excitation resulting in light emission. Incident electromagnetic radiation like x-rays and gamma rays typically ionizes atoms to produce fast free electrons or creates electron-positron pairs, which ionize other atoms as they lose energy. Light is produced from excitation of the scintillator occurring within microns of the track of the generated particles. Charged particles, in contrast, interact directly with electrons in the scintillator resulting in a one-step process. Neutrons interact only through nuclear interactions and produce gamma rays by capture and inelastic scattering, which produce electromagnetic radiation and continue the process until the light is emitted [13].

In a scintillation detector, the signal shape is determined by the decay times of optical states. Before the light emitting states (holes) are filled, and decay, multiple decay paths with non-radiative energy transfer are involved. If either the electrons or the holes are trapped in a non-radiative state that retains these charges with a lifetime much larger than the decay time of the luminescence center, we obtain a slow component. The pulse shape has rise and decay edges as shown in Fig. 1.4, where τ_r and τ_d are the rise and decay time constants with an approximated form given by Eq. 1.4.

$$I(t) \approx I_0(e^{-t/\tau_d} - e^{-t/\tau_r}) \tag{1.4}$$

Scintillation and Cherenkov effect are light emission processes. However, the physical mechanism is completely different. Cherenkov light is only produced when the velocity of the particle is larger than the velocity of the light in the medium. Also, for particles traveling at velocities

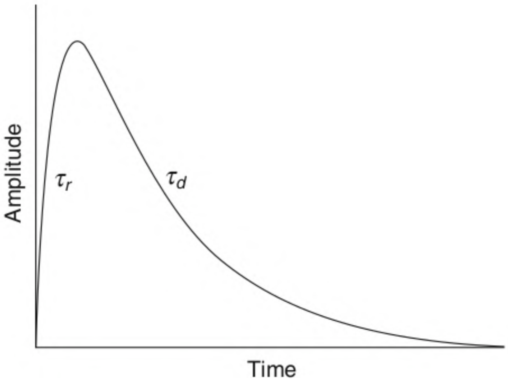


Figure 1.4: Typical scintillator pulse rise and decay time.

closer to the speed of light, the intensity of the Cherenkov light emission is typically lower than the light output of a good scintillator in a factor of 100 [14]. Cherenkov counters are challenging as they must detect single photons with high efficiency and little noise. Fast timing resolution is essential in time-imaging counters and is useful to reject background. Good segmentation in space may be needed to obtain adequate angular resolution in ring imaging counters (RICH) [15].

Cosmic Rays and Energy Response

A diverse range of Cherenkov counters is found in astroparticle physics experiments that study neutrinos, proton decays, gamma-ray bursts, and charged cosmic rays. There are different ranges of detectors, including calorimetric devices used to study nucleon decays, massive imaging detectors made of strings of photon detectors submerged in the sea, deep lakes, or polar ice cap, and detection of very high energy air showers either using large arrays of threshold Cherenkov detectors or stereoscopic air shower Cherenkov telescopes [16]. High energy cosmic rays energies can extend well above 10^{18} eV, and the interaction with the atmosphere generates air showers induced by both hadrons and gammas, which then can be captured by a detector. There are two different basic detector concepts to study these events: Cherenkov photons directly produced by the shower in the atmosphere, and the second is to build a large array on the ground to sample the particles produced by Extended Air Shower (EAS) that reach the ground (Fig. 1.5). Land observatories like the Latin American Giant Observatory (LAGO) [17], Piere

Auger Observatory [18], and The High-Altitude Water Cherenkov Observatory (HAWC) [19] consists in several water Cherenkov detector arrays to study these events.

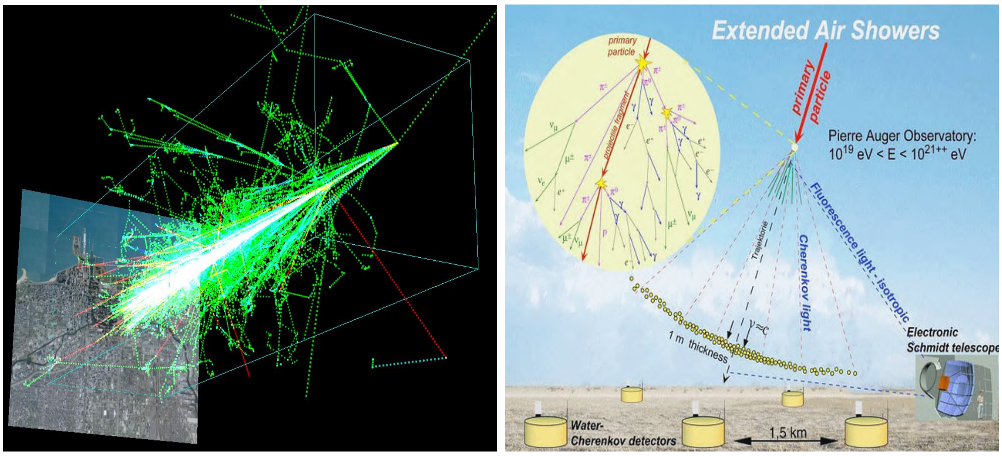


Figure 1.5: Example of extensive air showers produced by cosmic rays [20], [21]

Water Cherenkov detectors have different signal responses depending on the type of particle. Some of the different types of signals are listed below [22].

- Electrons usually drop all their energy in the detector, giving a signal proportional to their energy.
- Photons usually convert into an electron-positron pair within the water volume, and then the secondaries radiate all their energy. In the end, the signal is again proportional to the energy of the incoming particle.
- Muons, on the other hand, go through the detector without losing all their energy (except in the rare muon decay cases). The signal is then proportional to the track length in the detector and no longer to the particle energy.

Given that energy distribution for electrons and photons falls off as a power law, the signals from these particles in a WCD also fall off as a power law. On the other hand, given that the track length distribution for muons in a WCD is normally peaked at the height of the water volume (most muons traces are vertical), the signals of all muons will sum to give a hump in a signal histogram. This hump is determined only by specific characteristics of the detector (e.g., geometry, water purity) and electronics (photomultiplier tube gain) and allows a precise calibration point [22].

1.3.3 Semiconductors Detectors

Semiconductors detectors are capable of much higher energy resolution. These detectors are far more desirable for energy spectroscopy than gas-filled or scintillation detectors. This improvement is primarily due to the better statistics regarding the number of charges excited by radiation interaction. On average, it only takes 3 to 5 eV to produce an electron-hole pair in a semiconductor. By comparison, it takes between 25 and 40 eV to produce an electron-ion pair in a gas-filled detector and between 100 eV and 1 keV to produce one photoelectron [23]. There are many types of solid-state detectors [24], and all of them have specific working principles that are out of the scope of this thesis. In a very simplified way, semiconductor detectors operate on the principle of induced charge, in which mobile charges drifting through the detector cause charge to flow in an externally connected circuit. The detector produces current pulses that depend on the RC time constant of the output circuit. The voltage pulse induced by the detector begins to form immediately when the charges begin to move. Many electron-hole pairs excited in a detector induce a current according to the scaled motion of electrons and holes.

1.4 State-of-the-art of HEPD Electronics

This thesis proposes a front-end electronic readout system for HEPD based on SoC-FPGA to be used as a multichannel High Voltage Power Supply System (HVPSS) for MPGDs. The modular architecture of the design allows using it also as a DAQ for WCDs. In HEPDs readout electronics, SoC-FPGA devices have become extremely useful for building custom digital hardware to specific requirements, including non-standard data processing and interfaces. In June 2020, CERN accelerators were upgraded as part of scheduled Long Shutdown 2 (LS2). Several experiments took advantage of this opportunity to upgrade the electronics of their detectors to improve the data acquisition.

The JET calorimeter trigger system of ATLAS enhanced its electronics to exploit fine granularity readout using a new system of Feature EXtractors (FEX) with a latency budget of 400 ns in a Xilinx Ultrascale+ SoC [25]. CERN's new generation of radiation monitoring devices for radiation protection CROME (CERN RadiatiOn Monitoring Electronics) uses a fully reconfigurable 28 nm Xilinx Zynq SoC-FPGA for high-end embedded calculations, communication, and data storage [26]. The barrel of the CMS electromagnetic (ECAL EB) and hadronic calorimeters (HCAL HB) new DAQ tests include Zynq SoC-FPGA to meet the required specifications [27]. These are some upgrades scheduled for the LS2, leaving no doubt about the importance of SoC-FPGAs in the context of HEPDs.

1.4.1 High Voltage Power Supply System for MPGDs

The power supply system is essential in most experiments. Commercial manufacturers like CAEN [28] provide sophisticated HV power supplies used for the CMS tracker system [29]. CAEN offers a Universal Multichannel System up to 3.5 kV providing a maximum current of 3.5 mA, up to 10 nA of the current set and 500 pA of current monitor resolution, 5 mV of voltage monitor resolution and 2 different channel grounding [30]. Devices like AG7435 provide up to 24 HV channels and 1 nA of maximum current resolution [31].

Commercial products provide multiple solutions for HEPDs, but with the increase in complex detectors, custom solutions are needed. Radiation tolerant programmable power supply for beam screen heaters of LHC has been developed using Microsemi anti-fuse A54SX72A FPGA as the main component of the cryogenic system control [32]. The FPGA provides a range controller, clock generation, and 14-bit ADC to measure the output of the temperature sensor in a heavy radiation environment. In 2019, Korea Superconducting Tokamak Advanced Research (KSTAR) upgraded the power supply system of their electron cyclotron (EC) [33]. The EC integrated control system has a built-in FPGA whose main role is to control the high voltage power system to keep the RF-beam quality. The new EC control system replaces PLC-based electronics to favor real-time monitoring with a processing cycle of 1 μs and turn-off time of 2 μs.

In the context of MPGDs, the high voltage power supply system requires fast transient analysis with time resolution $\leq$ 5 ns, current measurements $\leq$ 10 pA at a sampling rate of 100 kHz, 20 mV of voltage resolution, and user-defined actions for pre-breakdown conditions. Hybrid MPGDs gain depends on the relative HV applied between its electrodes instead of an absolute reference implying several HV power domains adding another layer of complexity to the design (more details in Chapter 3).

1.4.2 Data Acquisition System for WCD

The second application described in this thesis is a DAQ for WCD in the context of cosmic rays studies. As mentioned in Section 1.3.2, ground observatories such as Pierre Auger have 1660 surface detector stations to study cosmic rays and gamma-ray burst. The bandwidth of the front-end electronics board is set to 180 MHz to determine the pulse width. Signal sampling is performed by ALTERA Cyclone III series FPGA, taking 6.4 μs of data samples, 1.6 μs before, and 4.8 μs after the trigger [18]. A discrimination logic tags the samples depending on whether the incoming signal was above or below a programmable threshold. In 2018 an upgrade of the stations was done, adding plastic scintillators (SSD) on the top of each surface detector called AugerPrime [34]. The local trigger and processing capabilities were increased by using a more powerful local-station processor and FPGA, allowing the implementation of new triggers combined with SSD and WCD triggers in addition to the current ones. The recorded traces are digitized with a sampling frequency of 200 MHz and are digitally filtered and down sampled at 40 MHz. The timing accuracy is improved to 2 ns thanks to the implementation of a new GPS receiver [35].

The TAIGA (Tunka Advanced Instrument for cosmic ray physics and Gamma Astronomy) observatory addresses ground-based gamma-ray astronomy at energies from a few TeV to several PeV. In 2020 a one square kilometer setup was put into operation [36]. The observatory consists of wide-angle Cherenkov detectors and Imaging Atmospheric Cherenkov Telescopes (IACT) of electron and muon detectors grouped in three jointly operating arrays. The camera signal processing system consists of a MAROC3 ASIC amplifier-shaper comparator that detects signals from 28 PMTs, DC anode currents, and high voltage control. The charge of the pulse is stored in a buffer and transferred to an analog multiplexed output that comes to an external 12-bit serial ADC. The trigger signals are fed to the FPGA to form the cluster local trigger according to the specific number of received trigger signals within a 15 ns interval. A diagram of the TAIGA signal processing system is shown in Fig. 1.6.

1.5 Summary

This chapter introduces the basic working principles of the physics behind the most common types of High Energy Particle Detectors (HEPDs). A brief explanation of the interaction of

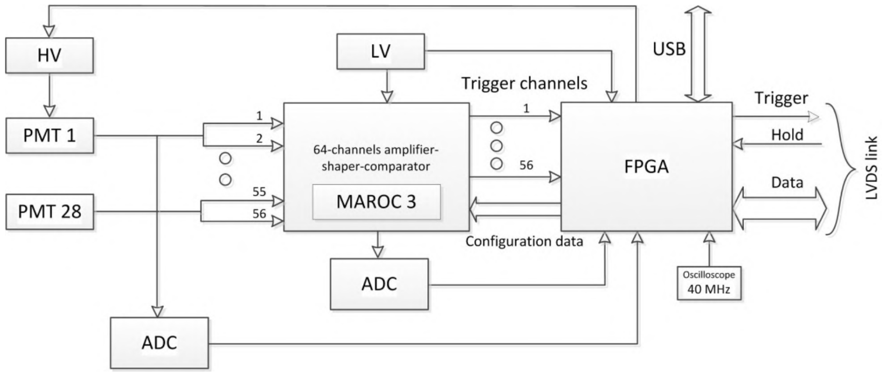


Figure 1.6: Block diagram of TAIGA signal processing system with MAROC3 ASIC [36].

the particles with matter is presented to introduce some concepts used in further chapters of this thesis. It is also explained the typical components of modern electronics for HEPDs and the use of SoC-FPGA in these architectures. Finally, it is presented a showcase of the state of the art applications of electronic systems based on SoC-FPGA in HEPDs and for the two specific cases of study, HVPSS for MPGDs and DAQ for WCD. The next chapter describes the concepts of the hybrid MPGD detector used for the RICH-1 in the COMPASS experiment and the requirements of the electronics to develop the HVPSS.

Chapter 2

Ring Image Cherenkov Detector (RICH-1) for COMPASS Experiment

The Common Muon and Proton Apparatus for Structure and Spectroscopy (COMPASS) is a high-energy physics experiment sited at the Super Proton Synchrotron (SPS) of the European Organization for Nuclear Research (CERN), Geneva, Switzerland. The experiment aims to investigate hadron structure and hadron spectroscopy with high-intensity muon and hadron beams.

The COMPASS experiment was proposed in 1996 and approved by the CERN research committee in 1997-1998. The experiment was set up between 1999 and 2001, and finally, in 2001, the first commissioning run was performed. Until the start of the LHC experiments, COMPASS was the largest data-taking experiment at CERN. It is also a pioneer in adopting new detector and readout technologies, such as MicroMegas, GEM detectors, and most recently, THGEM photon detection [37].

A second phase started in 2012 to study the transverse and 3D structure of nucleons using Deeply Virtual Compton Scattering (DVCS), Hard Exclusive Meson Production (HEMP), SIDIS, and polarised Drell-Yan (DY) reactions [38].

The layout of the COMPASS spectrometer is shown in Fig. 2.1. Multiple detectors along a 50 meters path are used for the studies proposed during Phase II. In the following sections, the main focus will be the Ring Image Cherenkov (RICH-1) Detector, which is the development target described in this thesis.

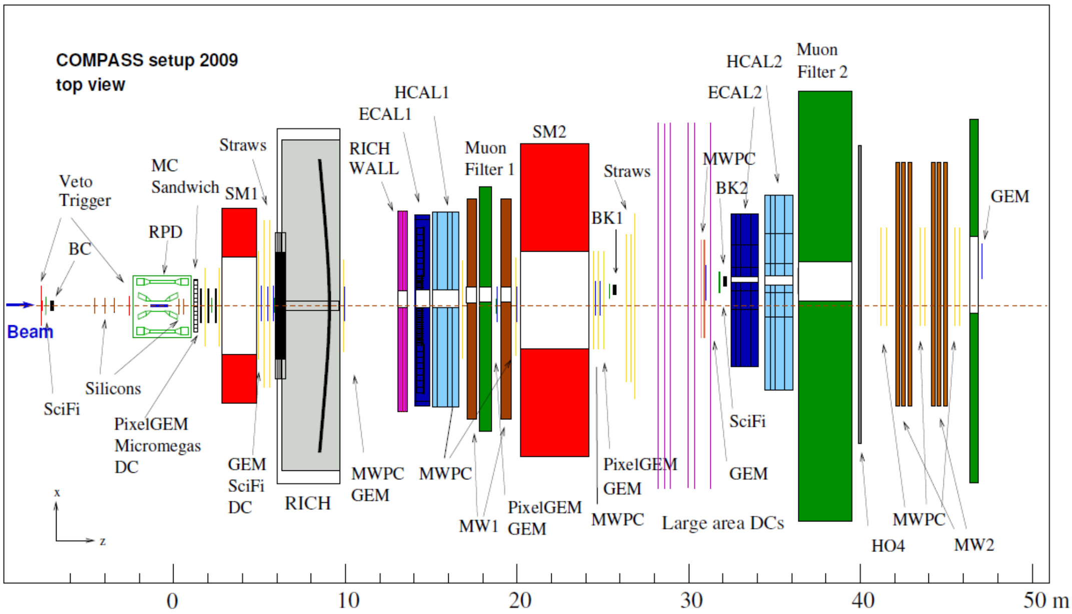


Figure 2.1: Top view of COMPASS spectrometer in 2009 (for detector names, see text).

The SPS M2 beamline consists of an approximately 600 meters long pion and kaon decay channel. The remaining hadrons are observed in up to 9.9 meters of Beryllium. The maximum momentum is 280 GeV/c with maximum intensities for 10^{12} incident protons at 400 GeV/c.

2.1 The RICH-1 Detector

The RICH-1 (Ring Image Cherenkov Detector) is one of the key detectors of the COMPASS experiment. It is designed to perform π/κ separation up to 60 GeV/c in a high-intensity environment. It is a large acceptance gaseous RICH with 3 m long C_4F_{10} radiator at atmospheric pressure, maintained at 25^o to obtain uniform temperature in the radiator volume [15]. An artistic representation of the COMPASS RICH-1 is depicted in Fig. 2.2 (right).

Cherenkov rings produced by the particle interactions with the gas are shown in Fig. 2.3. The ring's diameter depends on the particle's energy following Eq. 1.1.

The pixel segmentation of the photocathodes (pixel size: 8x8 mm^2) results in about 83000 channels equipped with analog readout electronics (mainly needed to obtain good efficiency). The expected occupancy level is 85% resulting (at a maximum trigger rate of 10^5/s) in a total

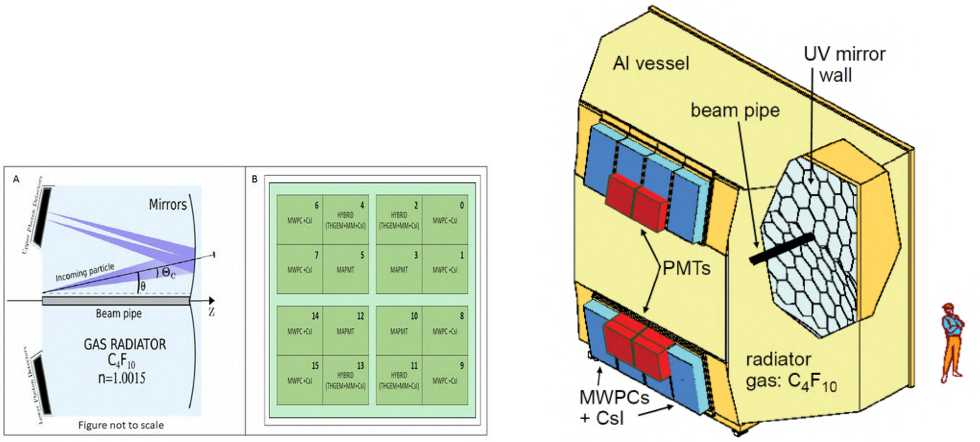


Figure 2.2: Artistic representation of COMPASS RICH-1 Detector depicting the placement of the Photon Detectors in blue color.

maximum data flow of 2.5 Gbyte/s. During the first phase of the experiment, the heart of the RICH-1 readout system was the large front-end BORA boards housing the front-end chip and local intelligence based on FPGA (Xilinx Virtex XCV100) for logic control of the front-end stage and data pre-reduction [39], [40].

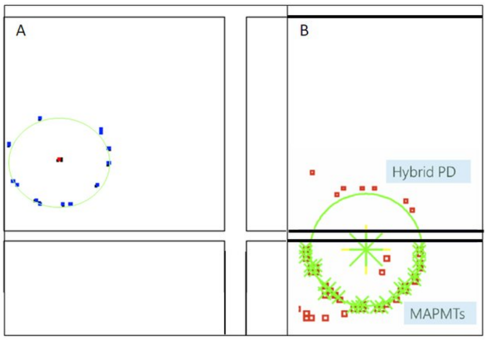


Figure 2.3: Cherenkov rings produced by the reflection of the photons from the mirror wall.

Three photo-detection technologies are used in the RICH-1: Multi-Wire Proportional Chambers (MWPCs) with CsI photo-cathodes, Multi Anode Photo-Multipliers Tubes (MAPMTs), and Novel Micro Pattern Gaseous Detectors (MPGDs). The whole photo-detection surface was originally equipped with 16 MWPCs of 600 X 600 mm^2 active area. However, these detectors have limitations in terms of time resolution, maximum effective gain ($\approx 10^4$), time response

($\approx \mu s$), rate capability, and lifespan of the CsI photo-cathodes.

In 2006 four central chambers were replaced with detectors consisting of MAPMTs coupled to individual fused silica lens telescopes, as shown in Fig. 2.2 (left). These detectors have excellent time resolution, and it is possible to cope with the high particle rates of the central region [41]. In parallel, an extensive R&D program to develop a Thick-GEM-based photon detector for large areas [42] established a novel hybrid technology combining Micromegas (MMs) [43] and THick Gas Electron Multipliers (THGEMs) [44].

In 2016 the RICH-1 was upgraded by replacing four of the remaining twelve MWPCs with new detectors based on the novel hybrid MPGD technology [45].

2.2 The Hybrid Detector Architecture

Fig. 2.4 depicts the basic structure of the hybrid MPGD detector. Two layers of THGEMs and a final MM work as electron multiplication layers, drift and mesh wires, and the bias voltage between layers works as transfer layers for the electrons. The bias voltage in the multiplication layers is applied through its electrodes. Each MPGD hybrid arrangement has six bias voltage electrodes and one connected to the ground. The first electrode is connected to the "DRIFT" wires producing the first transfer layer. Each THGEM has two electrodes: "TOP" and "BOTTOM". The MM's "MESH" is usually referred to ground and a positive voltage in the "PADS" creates the final multiplication layer before the readout. Light sensitivity is obtained via a thin (300 nm) CsI film deposited on the top of the first THGEM electrode, acting as a reflective photo-cathode to produce the first electron avalanche.

A brief description of the critical parts is presented in this section.

2.2.1 Thick Gas Electron Multipliers

THGEMs are electron multipliers derived from the Gas Electron Multipliers (GEM) design. GEMs are constructed of 50-70 micrometer thick Kapton foil coated in copper layers and 30-50 micrometer diameter holes done by photolithography and acid etching. THGEMs scale the geometrical parameters by replacing the fabrication technology with a standard printed circuit board (PCB) and drilled holes. Similar to the GEMs, the hole arrangement is a repetitive pattern in an equilateral triangle [46].

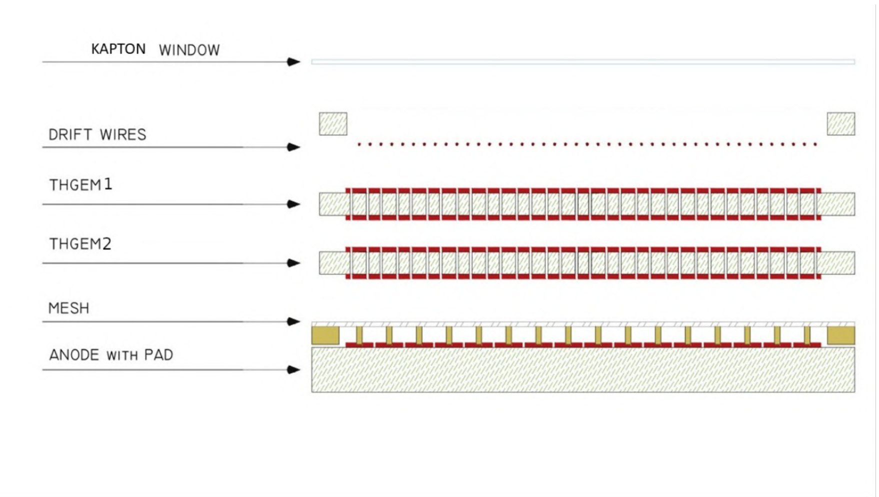


Figure 2.4: MPGD hybrid arrangement with two layers of THGEMs coupled to a MM (Mesh) on a pad segmented anode (not to scale).

Typical values of the geometrical parameters are PCB thickness of 0.4-1 mm, hole diameter ranging between 0.3 and 1 mm, and hole pitch of 0.7-1.2 mm, as shown in Fig. 2.5. The conical shape of the GEM holes that forms an uncoated polyamide ring is replaced by a clearance rim.

The gain stability in time strongly depends on the rim size [42]. Gain variations $\leq 20\%$ when the rim is absent, whereas huge variations are observed when the rim is large (0.1 mm). The gain increases with the rim size and with the PCB thickness. No rate dependence of the gain up to rates of at least 100 kHz/mm^2 has been observed. Large gains above 10^5 have been reported for detectors with three or four layers of THGEMs.

The THGEMs can be built in large series and sizes using standard PCB techniques. However, the process needs to be optimized to satisfy the requirements to be used for photon detection. A detailed summary of the different THGEM production procedures for COMPASS is described in the Ph.D. thesis of Shudha Dasgupta [47].

2.2.2 Micromegas Photon Detectors

Micromegas stands for Micro-Mesh Gaseous Structure. It is a gaseous particle detector from the wire chamber's development. Micromegas are a miniaturized version of a very asymmetric two-stage parallel plate detector. A micromesh separates the conversion space of about 3 mm

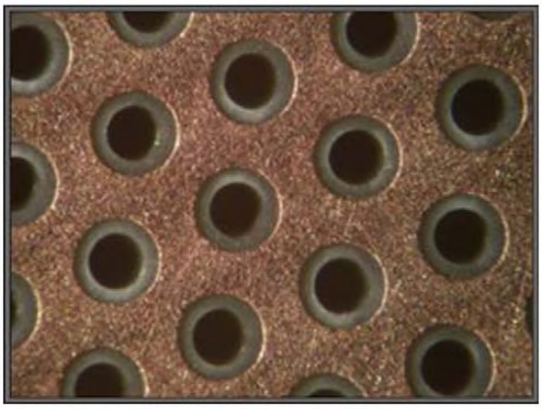


Figure 2.5: Image of a THGEM with holes of 0.3 mm diameter, the pitch of 0.7 mm, and rim size of 0.1 mm

for a small amplification gap that can be as small as 100 μm [43].

Fig. 2.6 describes the representation of a typical detector. A particle crossing the MM ionizes the gas atoms creating an electron/ion pair (1). The produced electron drift towards the mesh due to the HV electrical field (2). Applying proper voltages to the electrodes produces a very high electric field in the amplification region (about 100 kV/cm). For large electrical field values, most conversions pass through the hole of the micromesh and directly reach the stripe anode electrode (3). The HV field accelerates the electron, creating an avalanche (4). The charges produced by the avalanche are collected by the strips and sent to the readout electronic (5).

The MMs have a gap of 128 μm; they are built by the MM bulk technology [49]. The Micromegas PCBs are based on the capacitive/resistive concept: the signal generated on the anode pad is transferred capacitively to a second pad for readout. The two pads are separated by a fiberglass layer 70 μm thick. Each anodic pad induces the signal from the MM to an embedded pad buried inside the PCB, which is connected to the front-end readout. The pad structure and the equivalent circuit's schematic are shown in Fig. 2.7 .

2.2.3 The Hybrid Micropattern Gaseous Detector Working Principle

MPGDs are operated with $Ar : CH_4 = 50 : 50$ gas mixture. The drift plane is installed at 4 mm from the CsI coated THGEM and is biased to a suitable voltage to maximize the extraction

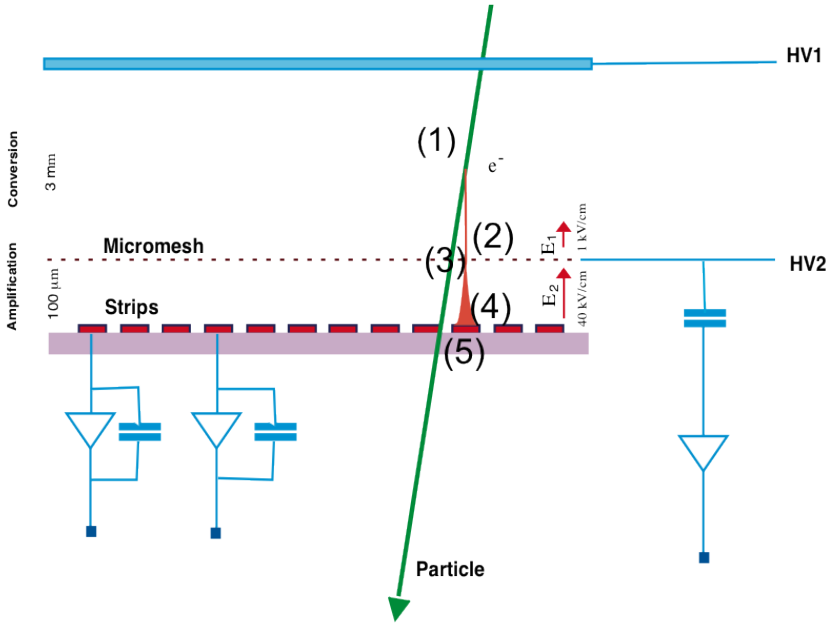


Figure 2.6: Working principle of a MM detector [48].

and collection efficiency of the converted photo-electrons [46].

The photo-electron converted on the CsI surface is guided into the electric field of one of the holes of the first THGEM, producing the first avalanche. The electric field accelerates the electron cloud across the 3 mm transfer region to the second THGEM. The misalignment of the holes with respect to the first THGEM ensures the charge is distributed among three holes and undergoes a second multiplication process.

The charge is guided by the electric field across the 5 mm gap to the bulk MMs where the last multiplication occurs. The MMs mesh is kept at ground potential while the anode, segmented in square pads of 7.5 x 7.5 mm^2 with 0.5 mm inter-pad gaps, is biased at positive voltage.

The typical voltage applied to the multiplication stages is 1270 V across THGEM1, 1250 V across THGEM2, and 620 V to bias the Micromegas. The drift field above the first THGEM is 500 V/cm, and the transfer field between two THGEMs is 1000 V/cm. The effective gain values for the three multiplication layers are around 12, 10, and 120.

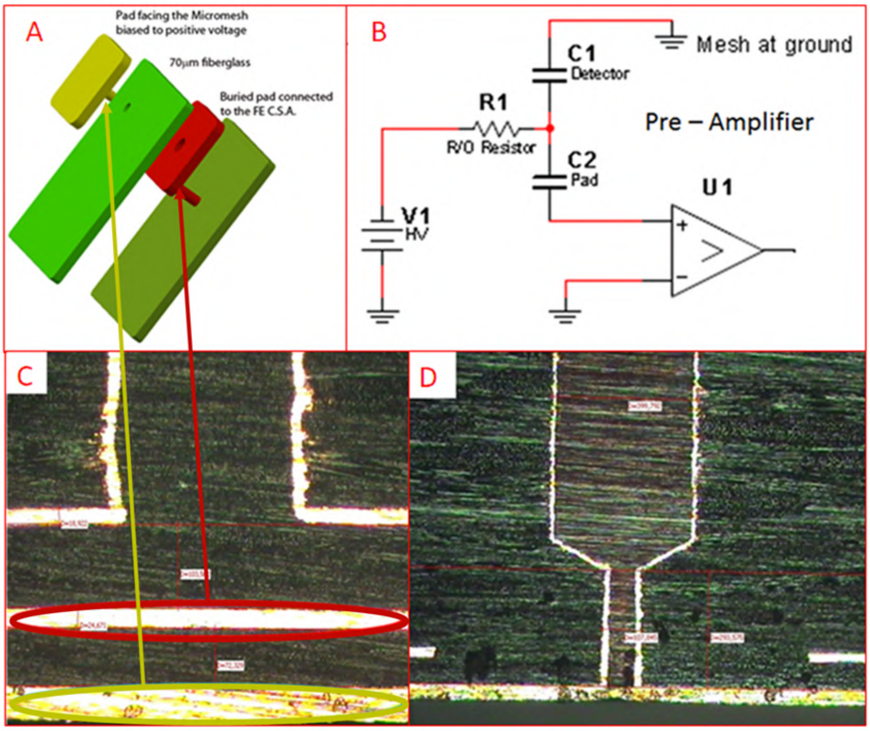


Figure 2.7: A: Single readout pad structure. B: The equivalent circuit diagram of the pads showing the resistive/capacitive anode concept. C and D: Metallographic section of the PCB [45].

A test prototype of a hybrid detector was designed and built. This prototype reproduces the hybrid MPGD implemented for COMPASS RICH-1. It has an active area of 10 x 10 cm^2, an anode segmented in 1024 square pads having a 3.5 mm pitch. The prototype, called minipad, is fully modular with front-end electronics and almost all services contained in the design. The internal structure of the minipad is shown in Fig. 2.8.

The prototype was tested at INFN Trieste laboratories and in a test beam at CERN SPS. Cherenkov rings have been observed for different CH_4 rich gas mixtures as shown in Fig. 2.9.

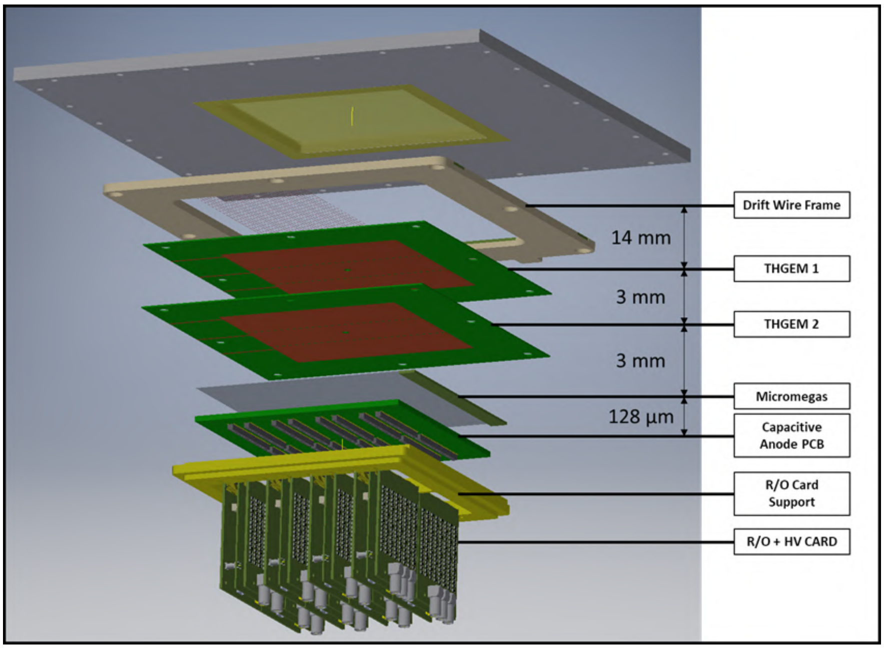


Figure 2.8: Detailed view of the Minipad MPGD hybrid schematic. [41]

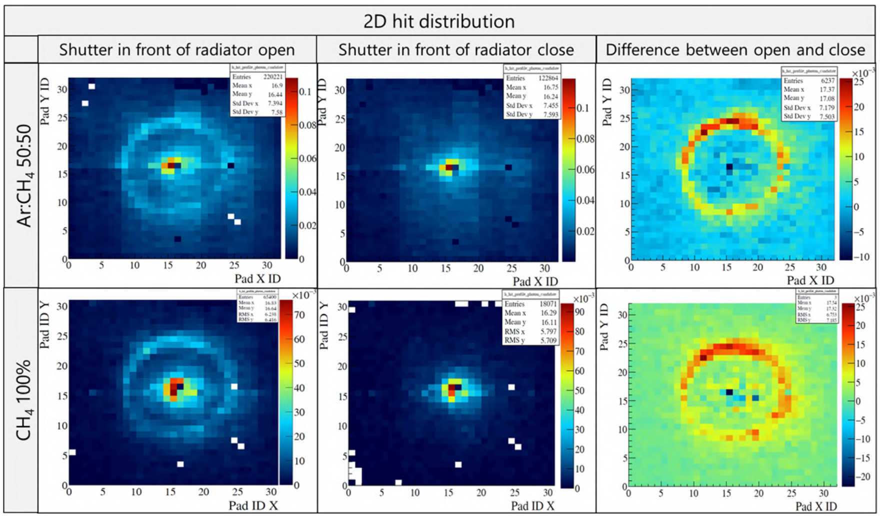
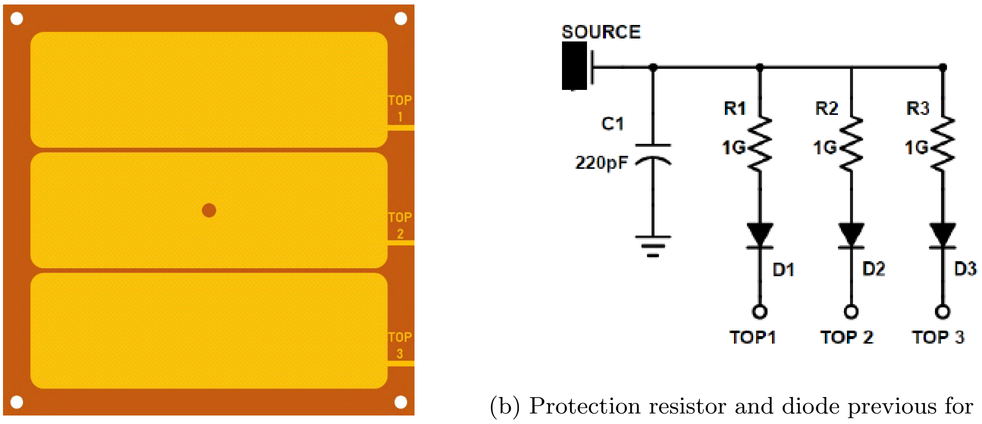


Figure 2.9: Observed Cherenkov rings in AR : CH_4 50:50 gas mixture and in pure CH_4 gas. More information available in [41].

2.3 The High Voltage System Requirements

An essential tool for the detector commissioning is the High Voltage (HV) control system which also allows for voltage and current monitoring and data logging. Each electrode needs to be polarized by a HV channel. Each THGEM, at the same time, is divided into independent sectors thanks to resistors, as shown in Fig. 2.10a. Fast diodes prevent current flow from one segment to another in case of electrical discharges (Fig. 2.10b).



(a) Sector division.

(b) Protection resistor and diode previous for three sectors on THGEM.

Figure 2.10: THGEM sector division with its corresponding protection

The requirements for the HV system originate from the unique requirements related to MPGDs in general and from the novel architecture of the detector. Current monitoring with fine resolution is needed to control MPGD operation.

Each amplification region depends on the relative voltage applied between the cascade electrodes. The three amplification regions need a relative voltage between them for transferring the charges, which implies that the HV applied to the electrodes is highly correlated. The electrodes segmentation adds further elements of complexity to the HV power supply system. The complexity of the system needs an automated control to prevent errors by the operator. Each stage's gain also depends on the temperature (T) and pressure (P), and it is amplified in a multistage detector. The HV power supply needs to provide active TP compensation and other misbehavior of the detector. The system also requires to provide logs of the relevant parameters, namely voltages and currents supplied by the HV units [50].

2.3.1 Hardware Components of the RICH-1 HV System

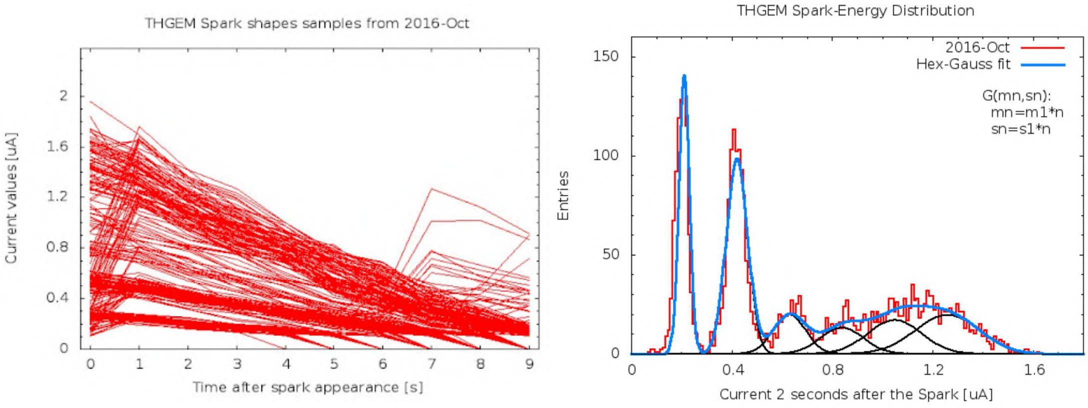
The current HV power supply is based on CAEN HV multichannel modules A1560H and A7030DP ([51], [52]) to polarize the THGEMs and the MMs, respectively. A SY4527 mainframe controls both modules [53]. The control and monitoring options are done via a Gigabit Ethernet interface.

The most relevant features of the A1560H units are the low voltage ripple, typically 20 mV pp from 10 Hz to 100 MHz spectrum at full load, fine voltage resolution of 100 mV for setting, 20 mV for monitoring, and 500 pA for current monitoring. These figures are quoted in the specifications and confirmed in operation.

MM pads are supplied by A7030DP with a maximum voltage of + 3 kV fully floating. The noise figures are < 15 mV. The voltage resolution is 50 mV for setting and 20 mV for monitoring. These modules offer less fine current resolution which is 2 nA for monitoring.

Sparks in the hybrid MPGDs installed in RICH-1 result in short current spikes. The power supply provides a readout with 1 Hz. MM spikes have a duration of $\approx$1-2 s, while THGEM spikes last $\approx$10 s. The order of magnitude of these recovery times corresponds to the time required for loading the equivalent RC circuit.

The sparks can be correlated among the different multiplication stages of a detector. Sparks in the two THGEM layers of a sector are 100 % correlated. This is expected considering that a spark results in a temporary short between the two THGEM electrodes, with a drastic local variation of the electric field that also affects the other THGEM layer. The spark rate in MM is low compared to the THGEMs. MM sparks are accompanied by sparks in THGEMs in 70 % of the cases [50]. There are also expected sparks between neighboring sectors, mostly one or two segments, but they can propagate to the whole THGEM. Fig 2.11a shows the time after sparks appear in seconds versus the current values in the THGEM detector. The maximum current drain happens between 1 and 2 μs. By analyzing the values of the current two seconds after the spark (Fig. 2.11b), it is noticeable that two peaks near 0.2 and 0.4 μA and a non-negligible number entries above 1 μA. These values may indicate a correlation between the initial electrical discharge and subsequent ones. A higher monitoring rate may confirm this correlation, and with enough response time, the fast-transient propagation may be stopped.



(a) Spark shapes samples

(b) Spark energy distribution

Figure 2.11: THGEM sparks shapes samples and distributions obtained in October 2016. Analysis done by G. Hamar, presented at COMPASS CM, Nov. 2016.

2.4 Summary

The hybrid MPGD used on RICH-1 consisting of two THGEMs and one MMs increases gain and response time compared with the previous MWPCs. The THGEM-MM hybrid PD technology could be used for other applications, for instance, a RICH dedicated to Particle Identification (PID) of high momentum particles at the future Electron-Ion Collider (EIC) experiment [54], where higher spatial resolution of the PD would be needed.

A hybrid detector implies an increase in the complexity of the HV system. Commercial devices can provide a solution with a sample resolution of 1 Hz with current and voltage monitoring in the order of 1 μA and 20 mV, respectively. The hybrid MPGD needs high resolution current measurement in the order of pico-amperes to avoid error propagation through the gain stages. The HV power supply system of the detector requires to timestamp fast transient events with high resolution in the order of nanoseconds to study the evolution of electrical discharges between electrodes and sectors. The HV power supply system also needs to take preventive actions automatically anticipating breakdown conditions.

The next chapter describes the hardware design and development carried out in the framework of this thesis to solve the challenges given by the previous mentioned requirements. It is presented all the hardware modules comprising a HVPSS channel.

Chapter 3

The High Voltage Power Supply System Design for Micro-pattern Gaseous Detectors

The multi-channel High Voltage Power Supply System (HVPSS) presented in this thesis was built to meet the unique requests related to hybrid MPGDs. The multistage structure of these detectors imposes the need for highly correlated HV control applied to the electrodes in the two THGEMs and the MMs. The segmentation of the electrodes adds further elements of complexity to the HVPSS design.

In addition, changes in pressure and temperature actively affect the gain in gaseous detectors due to voltage variations. In a hybrid system, every variation is carried and amplified in each stage. The HVPSS includes environmental variables monitoring (e.g., temperature and pressure in the gas container) providing active compensation of the applied HV.

The system also requires running automatic protocols to react to the occasional misbehavior of the detector and log voltage and current supplied by the HV. A sample of fast transient phenomena like electrical discharges needs to be logged with high-resolution time stamping.

An accurate study of these transients can be used to prevent their propagation through other electrodes. Each electrode is connected to a HVPSS channel. A network interface provides communication among channels to make decisions depending on the information provided by the neighbors.

In summary, the HVPSS should meet the following requirements:

- Provides current measurements with 10 pA of resolution at 100 kHz.

- Performs real-time monitoring of the main parameters (voltage and current) to study the precise evolution of breakdown events.
- Performs nanosecond time stamping to study the evolution of fast electrical transients.
- Generates HV at detector level from 0 to -4000 V with 20 mV resolution.
- User defined actions for pre-breakdown conditions.
- The system must be modular and scalable, achieving nanosecond synchronization among channels in different HV power domain environments.

This chapter describes the hardware design and development carried out in the framework of this thesis to solve the challenges given by the previous mentioned requirements. It is presented all the hardware modules comprising a HVPSS channel. The hardware production was funded by the INFN-TS, COMPASS group, and MLAB-ICTP. The control firmware's specifics are described in Chapter 4.

3.1 The HVPSS Channel

Each HVPSS channel is divided into seven independent hardware modules, as is schematically shown with different colors in Fig. 3.1. The arrows indicate the interaction between the modules and the data flow. These hardware elements are:

1. HV DC/DC Supply board (Section 3.1.1) composed of the sub-modules:
    (a) HV DC/DC Converter
    (b) HV Control (Digital to Analog Converter (DAC))
    (c) Voltage and Current Monitoring (V_{mon} and I_{mon})
2. Picoammeter board (pA) (Section 3.1.2)
3. High-speed ADC board for data acquisition (Section 3.1.3)
4. Interposer board with HV Network Interface (Section 3.1.4)
5. Temperature and Pressure Sensors board (Section 3.1.5)

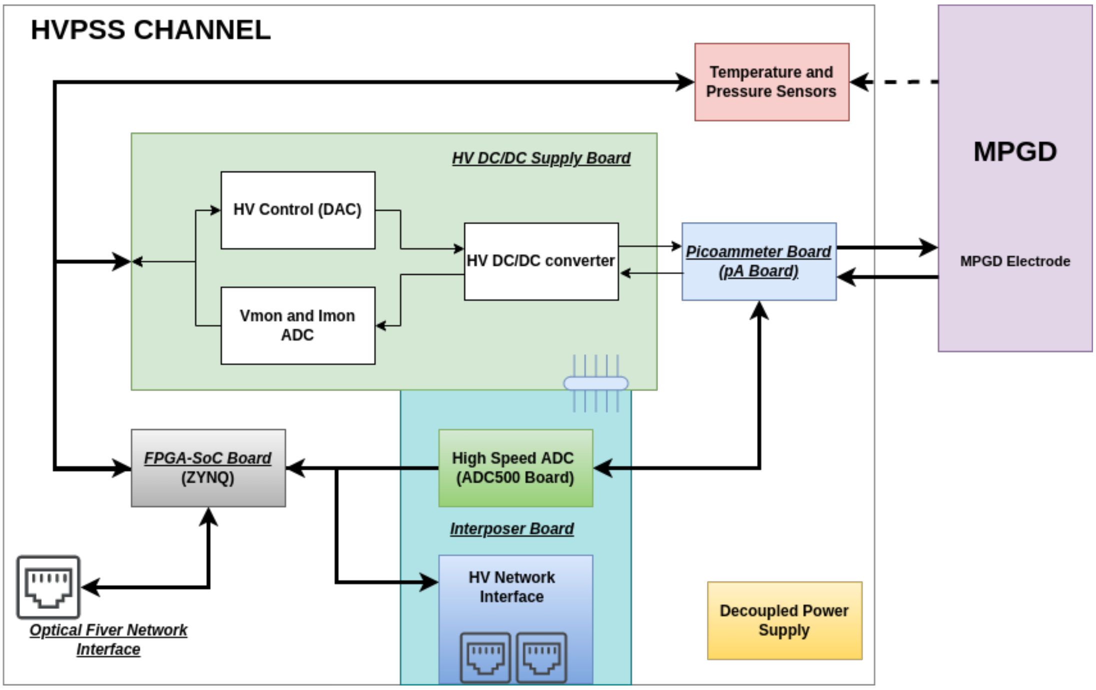


Figure 3.1: Block diagram describing the different hardware modules of the HVPSS channel.

6. Decoupled power supply (Section 3.1.6)
7. Data acquisition carrier based on a System on Chip (SoC) board (Section 3.1.7)

There are two main motivations for a modular design. The first is to ease the replacement with minimal intervention in case a component is damaged during operations. The second is the potential upgrade; if a more performing component is available, it is easier to upgrade a module without costly re-designs of the whole system. The following sections describe each hardware module and its interaction with the overall system.

3.1.1 The HV DC/DC Supply Board

A custom HV DC/DC supply board to provide the HV needed to polarize the electrodes was designed. The PCB provides a digital interface to control the HV DC/DC converter. Information on setup and monitoring is sent through a Serial Peripheral Interface (SPI) using HV isolation buffers to separate the power domains between the SoC-FPGA and the DC/DC

Converter. The following subsections detail the design process.

- The HV DC/DC Converter.
- HV Control (DAC).
- V_{mon} and I_{mon} readout.
- PCB Design and SPI Isolation.

The HV DC/DC Converter

The high voltage power supply selection is based on the following characteristics: compactness related to space requirements, capability to provide both positive and negative voltages, and low noise figure affecting the HV. An investigation of the market pointed to the best candidates EMCO Q60, A60, AG60 families, and BPS family by ISEG DC/DC converters. These devices need an analog input of 0 to 5 V to set up the output HV voltage. Some of these devices also provide a built-in voltage monitoring (V_{mon}) and current monitoring (I_{mon}) analog outputs for status control.

The market investigation has pointed out the candidate devices listed in Table 3.1, particularly EMCO [55] and ISEG [56] devices. The EMCO devices are more compact than the ISEG, as shown in Fig. 3.2.

Table 3.1: Main parameters of the candidate DC / DC converters produced by EMCO and ISEG.

DC / DC converter	**Producer**	**V_{Out}** [kV]	**V_{Ctrl}** [V]	**Power** [W]	**Ripple**	**Dimensions** [mm^3]
Q60-5R	EMCO	0 to +6	0 to +5	0.5	<1.0 %	13.72x13.72x13.72
Q60N-5R	EMCO	0 to -6	0 to +5	0.5	<1.0 %	13.72x13.72x13.72
A60P-5	EMCO	0 to +6	0 to +5	1	0.15 %	11.43x23.37x6.35
A60N-5	EMCO	0 to -6	0 to +5	1	0.15 %	11.43x23.37x6.35
AG60P-5	EMCO	0 to +6	0 to +5	1	0.3 %	17.50x26.70x6.35
AG60N-5	EMCO	0 to -6	0 to +5	1	0.3 %	17.50x26.70x6.35
BPn4010512	ISEG	0 to -4	0 to +5	1	<20 mV	40x50x17
BPp1010512	ISEG	0 to +1	0 to +5	1	<20 mV	40x50x17

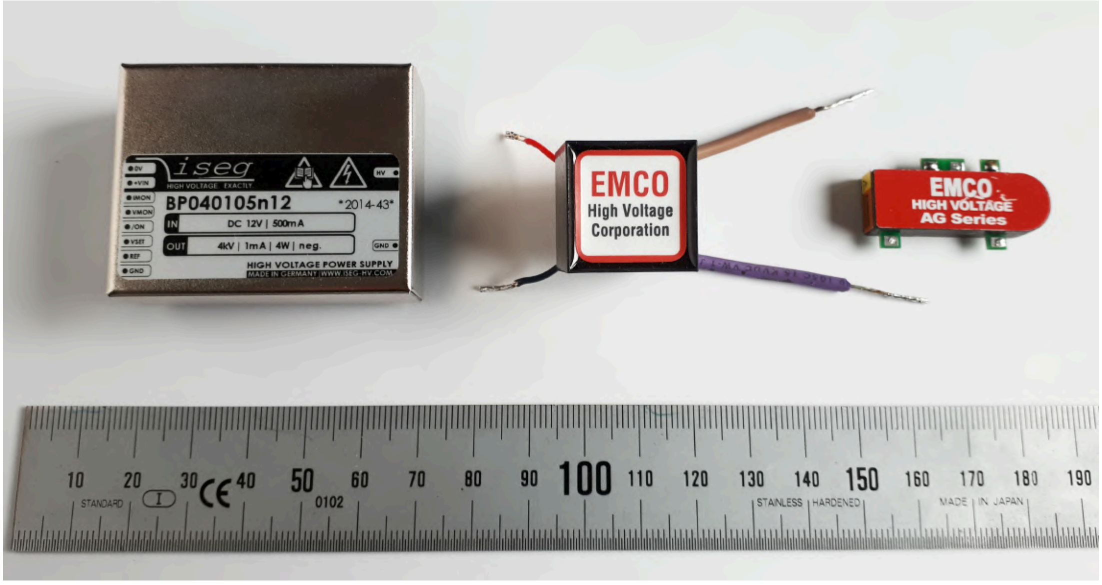
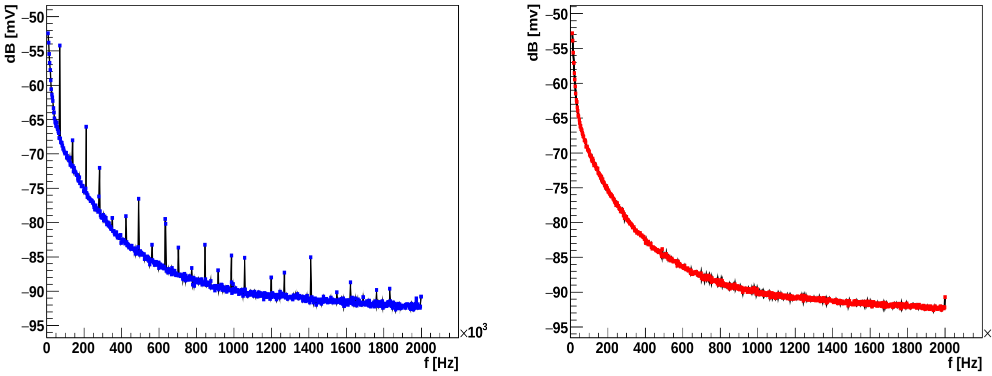


Figure 3.2: Image of some of the considered DC/DC converters studied: the BPn4010512 (left); the Q60-5R (centre); and the AG60P-5 (right).

A detailed study between the EMCO and the ISEG BSP family was done and shown in the paper ”A scalable High Voltage Power Supply System with system on chip control for Micro Pattern Gaseous Detectors” [57]. In this study, the entire Q60, A60, and AG60 families by EMCO as well as the BPS family by ISEG were tested with a 100 MΩ load. The minimum voltage output V_{out} indicated as V_{Th} of each device was measured via a HV probe FLUKE 80K-6. The low input control voltage (V_{Ctrl}) was measured via a multimeter.

The measured V_{Th} is 920 V for the Q60 devices, 1500 V for the AG60 devices, and 600 V for the A60 devices. The lowest output voltage was obtained for the ISEG converters with a minimum measured voltage of 1 V. It is important to remark that, during operation, all the EMCO devices exhibit discharge events with their frequency correlated to the device’s temperature, which increases during operation. No discharge events were detected for both of the ISEG converters.

Noise spectra analyses were performed using a spectrum analyzer with a 50 Ω terminated probe connected in series to the 100 MΩ resistor. The noise spectra refer to an output voltage of -4 kV for all the modules. A noise spectra comparison is provided in Figs. 3.3a and 3.3b for



(a) EMCO Q60N-5R

(b) ISEG BPn4010512

Figure 3.3: Noise power spectrum of the EMCO Q60N-5R (3.3a) and ISEG BPn4010512 (3.3b) converters operated at -4 kV output HV.

the converters Q60N-5R by EMCO and BPn4010512 by ISEG, respectively. The performance of the ISEG shows no observable noise peaks compared with the EMCO.

Despite the size, the ISEG devices provide voltage and current monitoring pins missing in the EMCO. The pin factor of the ISEG BSP family with standard 2.54 mm separation between pins makes them suitable to be placed in a socket simplifying the replacement in case of damage or change of polarity.

The ISEG BSP also has an internal reference voltage V_{ref}. The output voltage V_{out} changes according the setup voltage V_{set} with a maximum output V_{nom} with the following relation:

$$0 \leq V_{set} \leq V_{ref} \Rightarrow 0 \leq V_{out} \leq |V_{nom}| \pm 1\% \tag{3.1}$$

In particular, the BPn4010512 has a V_{ref} = 5 V and V_{nom} = -4000 V meaning that a V_{ref} = 2.5 V will produce a V_{out} = -2000 V ±1%.

The response characteristics of the selected converter were studied by measuring both the output voltage via a Lecroy PPE20kV HV probe and the output voltage of the V$_{mon}$ pin via a Keytley 197A $5\frac{1}{2}$ digit resolution digital voltmeter as a function of the applied V_{set} voltage. The last one is controlled via a 16 bit DAC MAX5216 (see section 3.1.1) where the Less Significant Bit (LSB) corresponds to a 300 mV variation of the HV output.

HV Control (DAC)

The output voltage of the ISEG DC/DC converter depends on the setup voltage applied in the V_{set} pin as stated in eq. 3.1. A 16 bits DAC MAX5216 [58] was selected to ensure repeatability of the output voltage. The device uses a precision external reference applied through a high resistance input for a rail-to-rail operation, ideal for handling the V_{set} and the V_{ref} of the BPS device. The MAX5216 reset the DAC output to zero at power up, providing additional safety.

The output is set using a 3-wire SPI with a maximum frequency of 50 MHz. This interface allows connecting the DAC with other components on the board. The analog output V_{out} for a code n and a reference voltage V_{ref} can be described by Eq. 3.2.

$$V_{out} = V_{ref}/65,535 * n \tag{3.2}$$

Since the DAC is rail-to-rail, we can obtain the HV output HV_{out} by substituting V_{ref} with the nominal voltage V_{nom}.

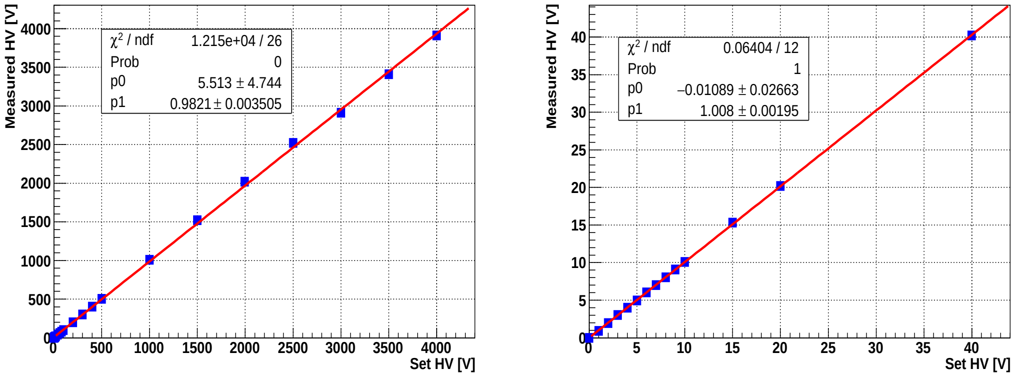
$$HV_{out} = V_{nom}/65,535 * n \tag{3.3}$$

For the ISEG BPn4010512, the minimum step is -61.03 mV, and the maximum integral nonlinearity (INL) is 8 LSB leading to a maximum deviation of the ideal output of ≈ -488.29 mV. A repeatability test was performed to verify this value. The test consists in setting a pre-defined DAC code corresponding to a well-defined HV output. The procedure continues by setting a sequence of random DAC values and power off and on cycles. The pre-defined DAC code is set back at the end of the sequence, and the HV output is measured. The difference between the HV outputs is used to define the voltage repeatability (V_{rep}). This procedure was performed with multiple values obtaining $|V_{rep}| \leq 400$ mV.

The device posses good linearity in the whole voltage range as shown in Fig. 3.4a for all range and in Fig. 3.4b for low voltages.

Voltage and Current Monitoring (V_{mon} and I_{mon})

The ISEG BPS provides voltage and current monitoring through the V_{mon} and I_{mon} pins. The analog signal needs to be digitized for active monitoring using an ADC. The Analog Devices



(a) 4 kV range exploration

(b) 40 V range exploration

Figure 3.4: Output voltage versus the control voltage for the BPn4010512 converter. The complete 4 kV range is explored (3.4a). The range up to 40 V is explored (3.4b).

ADC4002 was selected for its 18-bit resolution and 2 MHz sampling rate compatible with SPI [59]. Both monitors' coupling circuits are shown in Fig. 3.5.

The ADA4807 operational amplifiers are used as reference buffer and for signal conditioning. The voltage monitoring follows the rules of equation 3.3. However, the current monitoring depends on the maximum nominal current I_{nom}. For the BPn4010512 with 18-bit of resolution, the minimum V$_{mon}$ readout is of 15 mV and I$_{mon}$ readout of 3.81 nA.

PCB Design and SPI Isolation

The HV DC/DC supply PCB was designed to be used as a stand-alone module, as shown in Fig. 3.6. The digital signals are connected to an SFM connector or a standard 2.54 mm pin header compatible with a PMOD [60] interface, allowing to use either of the connectors with different carriers. The ISEG BPS DC/DC Converter is mounted on a socket to simplify the exchange of the module to be used with other polarities.

The PCB keeps the HV power supply in an isolated power domain (more details in Section 3.1.6). The SPI bus is isolated using the Texas Instruments ISO7841DWW, as shown in Fig. 3.7. An IIC bus is considered for future upgrades and to provide isolation of the pressure and temperature sensors.

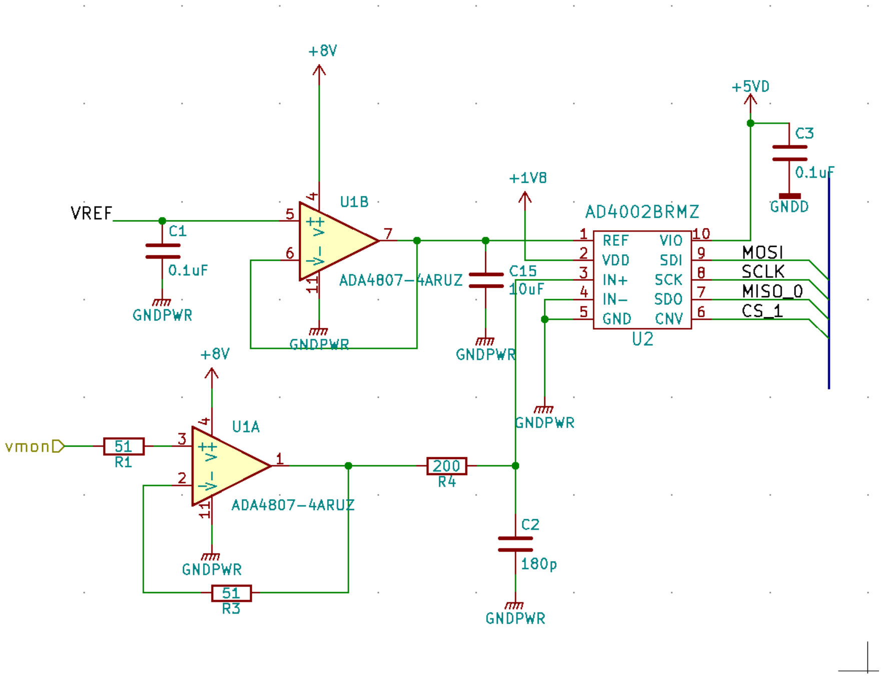


Figure 3.5: ADC4002 circuit with Analog Coupling

3.1.2 Picoammeter Board

As discussed in Section 3.1.1 the built-in current measurement can reach values in the order of nA. However, the system needs to provide measurements in the order of picoAmperes. The picoammeter board (shown in Fig. 3.8) is based on an operational amplifier in trans-conductance mode [61], [62]. The board is designed to directly measure the current on the electrodes, preparing the signal to be read by a high-speed ADC.

The first version of the picoammeter board was designed in collaboration between MLAB-ICTP and INFN-TS group in 2017 and tested with the first prototype of the HVPSS channel. The second version was designed in 2019 as part of this research program upgrading several components to improve the measurements. The new picoammeter board provides two different current scales digitally selected, fine offset, and coupling adjustments through digital potentiometers. The board also includes a high precision temperature sensor for drift compensation and a 10 kV 0C100HG HV optocoupler to apply fast-cut procedures on HV.

The output voltage V_o is related to the input current i_i by the relation shown in eq. 3.4.

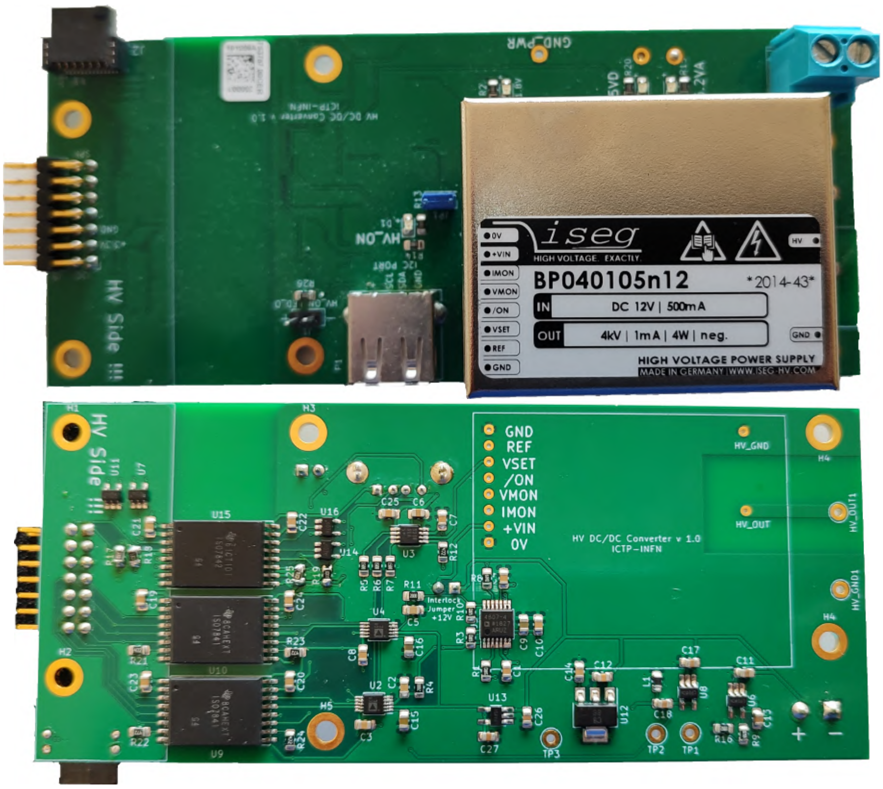


Figure 3.6: PCB designed for HV DC/DC Supply

The gain of the amplifier is directly proportional to the feedback resistor R_b. The basic circuit is shown in Fig. 3.9.

$$V_o = R_b i_i \tag{3.4}$$

An operational amplifier to be used in trans-conductance must have a high impedance differential input stage and low bias current. The AD549LHZ, by Analog Devices, meets these criteria with ultra-low bias current and 10^{15} Ω common-mode impedance [63]. The amplifier is coupled to a high precision 20 MΩ feedback resistor to define the current/voltage gain. The feedback resistor can be switched to a 4.4 MΩ using a relay to change the range in a 4.54 factor.

A digital potentiometer is used for the fine offset regulation (OFF_A and OFF_B in Fig. 3.10) and to match the ADC input range (AN_IN). The component selected was the AD5292 [64] with 10-bit resolution and 1% tolerance error. The potentiometer also has a 20-times programmable

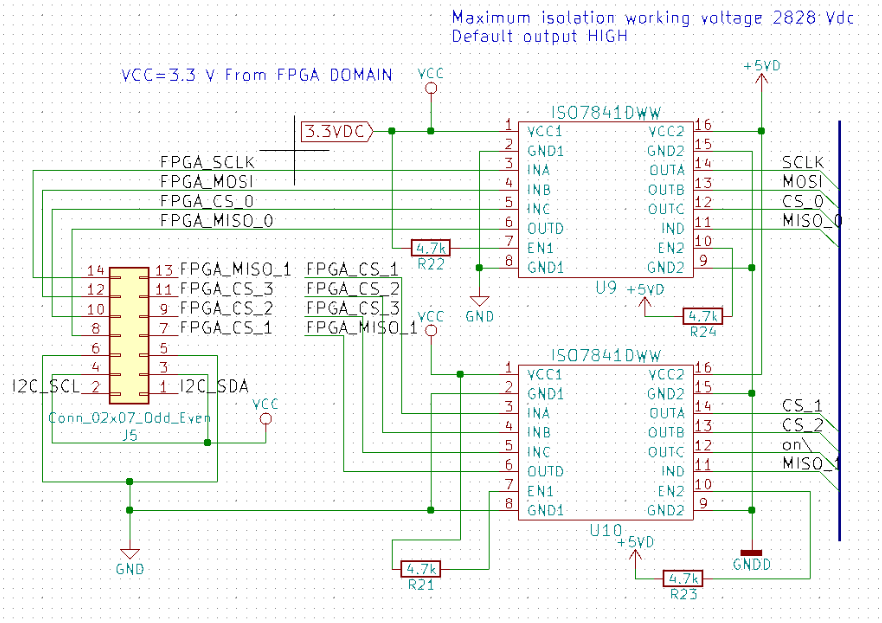


Figure 3.7: SPI Bus Isolation using ISO7841DWW

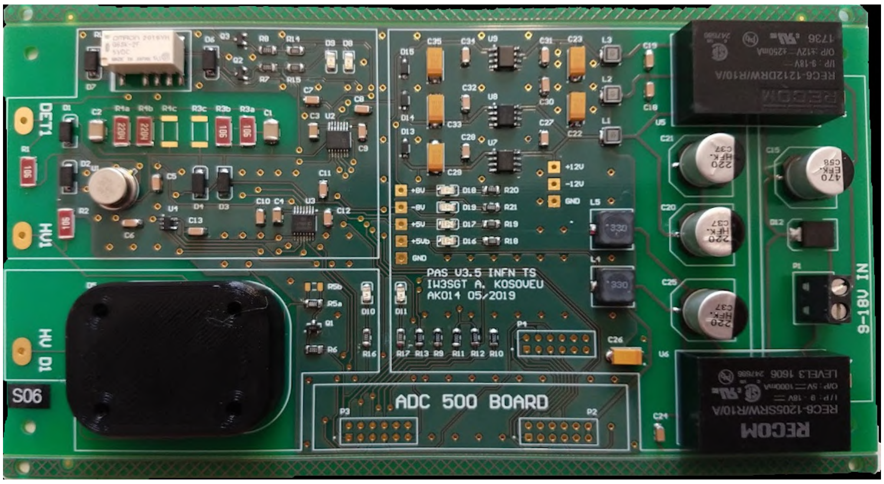


Figure 3.8: Picoammeter board version 2.0 compatible with ADC500 board

wiper memory to store pre-defined values. Two Zener diodes protect the operational amplifier. Several passive components have been added to protect the device from electrical discharges that may occur at the detector level to avoid possible damage.

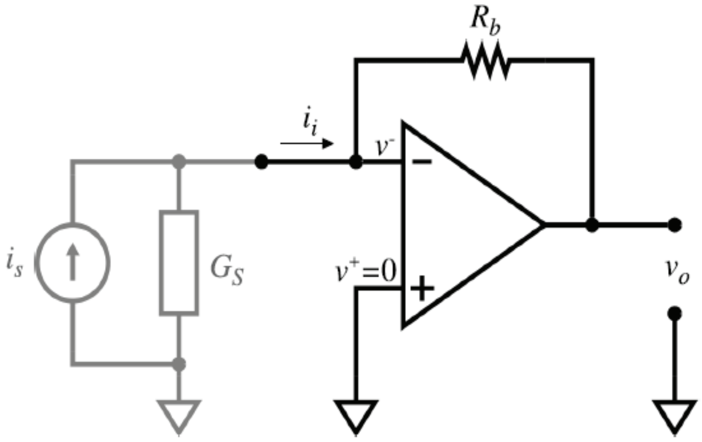


Figure 3.9: Operational amplifier in the trans-conductance scheme: operating principle

3.1.3 High-speed ADC Board for Data Acquisition

A high-speed ADC-based board was designed to digitize the analog signal from the trans-conductance amplification stage to measure the HV supply current. One of the requirements of the HVPSS is to detect fast transient phenomena, namely electrical discharges. A low power 8-bit 500 MHz ADC08500 analog to digital converter was selected to meet these requirements [65]. The ADC has a 1:2 demultiplexer read by 16 low-voltage differential signaling (LVDS) at 250 MHz.

The board was designed following the ANSI VITA 57 standard and equipped with a Low Pin Count (LPC) FPGA Mezzanine Card (FMC) connector. The ADC board shown in Fig. 3.11 includes self-calibration, fine input adjustment, full-scale range and offset, and multiple ADC synchronization capabilities.

Three onboard power regulators are implemented for low noise operation and circuit protection to avoid damages to the ADC due to out-of-range voltage spikes. The analog input is single ended, and DC coupled. A high-speed differential driver couples it with a common mode configuration.

An upgrade of the ADC500 board was done to include 16 General Purpose Input/Outputs (GPIO) for digital control on the picoammeter board (section 3.1.2). The GPIOs are mapped in two 8x2, 2.54 mm headers and directly connected to the FMC connector.

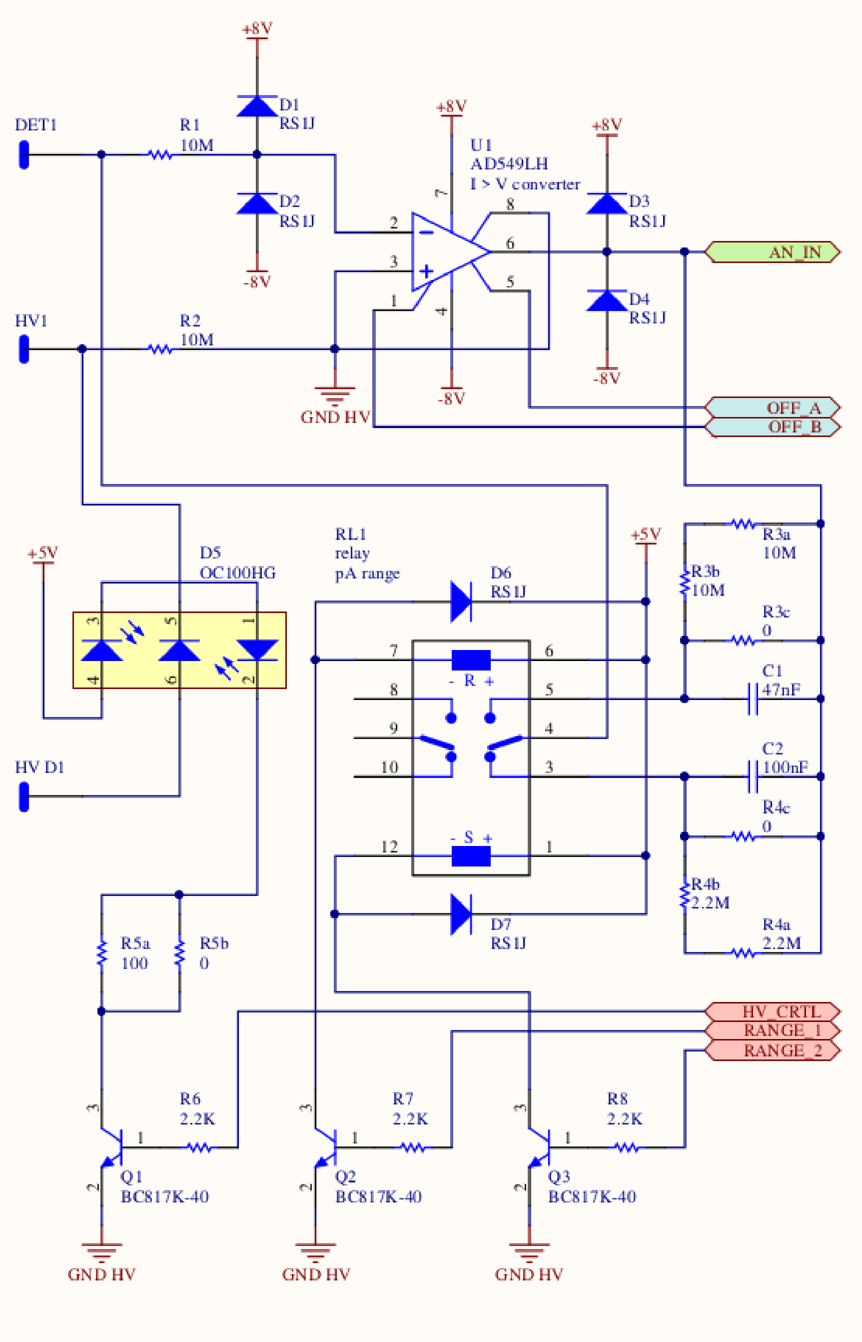


Figure 3.10: Trans-impedance configuration for AD549LHZ with two scales relay.

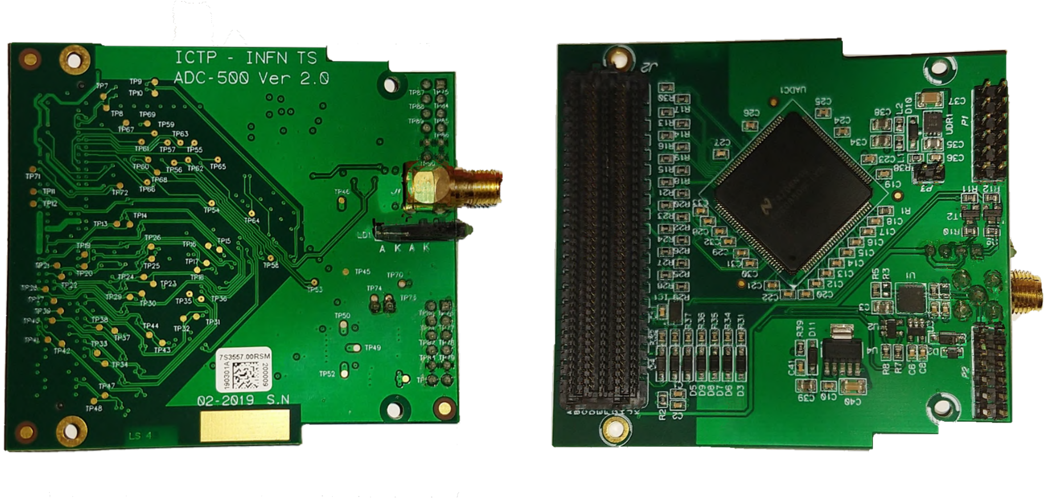


Figure 3.11: The ADC500 board (Rev 2.0) hosting the ADC08500, rear side (left) and front side (right).

3.1.4 Interposer Board

The interposer board provides extended interconnectivity from the FMC connector. It has four 2x13 block connectors and six high-speed differential pairs connected to a LEMMO connector. An 8-bit switch for address inputs. A TFM connector to couple the HV DC/DC Supply (section 3.1.1). Furthermore, a High Voltage Isolation Bidirectional Network Interface (HVIBNI) provides interconnection between HVPSS channels. The interposer board is shown in Fig. 3.1.4.

High Voltage Isolation Bidirectional Network Interface

Each channel must be connected in the HV power domain with independent floating power supplies to avoid electronic noise propagation in the detector. The absolute voltage among channels may be up to 2 kV, making a direct galvanic connection among them impossible. Wireless communication is not recommended to prevent electromagnetic noise induction in the detector; consequently, a HVIBNI for safe data transmission among multiple HVPSS control units was specifically designed. The HVIBNI interconnection topology is shown in Fig. 3.13.

Traditional circuit isolators, while effective, may not be suitable for the needs of the detector. Sustained HV DC decoupling is needed for prolonged times, and high-speed transmission

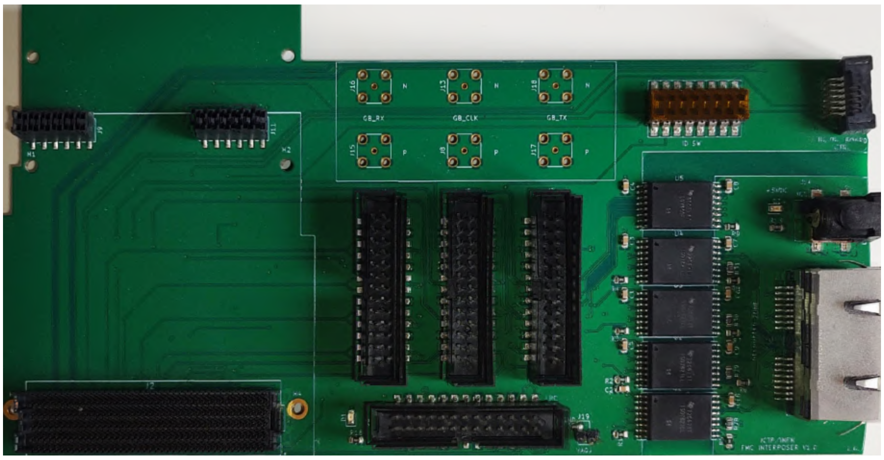


Figure 3.12: Interposer board

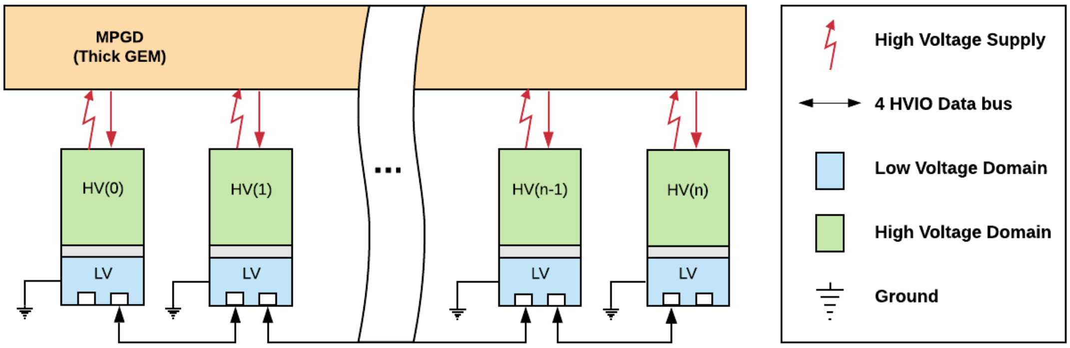


Figure 3.13: HVIBNI interconnection diagram

is preferred. Optical decoupling has several benefits, such as immunity to perturbing electromagnetic fields. However, achievable bitrates are typically limited [66]. For example, in the range of the fastest optocouplers, there are the HCPL-0723 and TLP2767, which can achieve 50 Mbps and up to 5000 V_{rms} decoupling for one minute; sustained DC voltage decoupling is only 500 V [67]. The inductive coupling has the advantage of differential transfer characteristics and high common mode noise rejection, but the main problem is the susceptibility to fast transient variations produced by spontaneous high voltage discharges [68]. Reinforced galvanic isolation can provide high data rates with a high isolation rating for DC voltage differences and transient peak surges protection up to 20 kV [69]. Among the commercial options available, the Texas

Instruments ISO78xx family of reinforced isolated buffers provides working high voltage DC isolation using silicon dioxide barrier (SiO_2) up to 2828 V_{DC}, 5700 V_{rms} for one minute and maximum surge isolation up to 8000 V [68].

The decoupling system consists of four LVDS isolated input/output (HVIO) buffers and is designed for bidirectional serial communication (Fig.3.14). In particular, each HVIO buffer is based on an ISO7821LLDW that has two LVDS buffers (receiver and transmitter), with a maximum signal transmission rate up to 100 Mbps [70]. A loop-back configuration was set to provide a bidirectional signal. Each power domain has input and output buffers controlled by two complementary enable signals. The FPGA is connected to the HV power domain with a local ground; this side is in charge of handling the input/output direction of the buffer. The transmission direction is set using an inverter gate connected to an ISO7840FDWW [71] buffer for decoupling. The low voltage domain has no control over the direction and is always referred to the global ground.

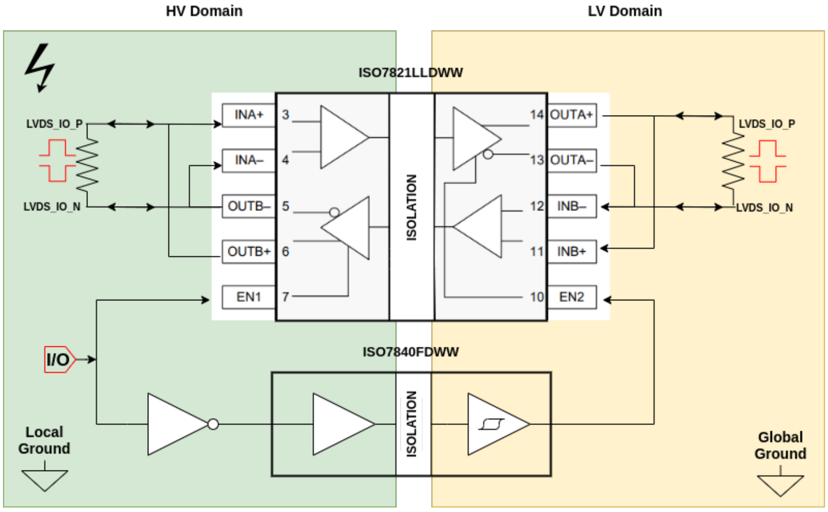


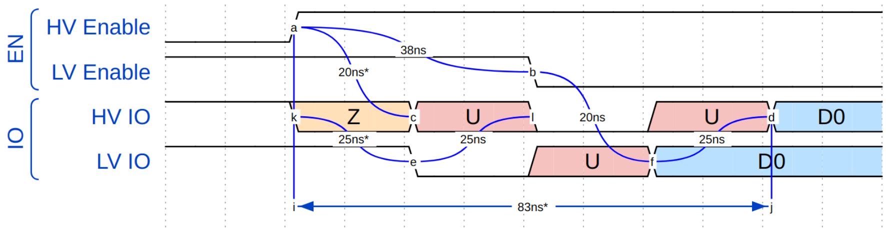
Figure 3.14: High Voltage Isolation Bidirectional Network Interface (HVIBNI)

Direction Switching Characteristics

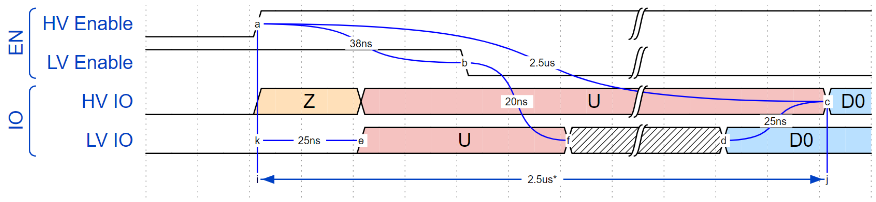
The time required for the enable signal to reach the output buffer to change from high-impedance to digital output is called enable propagation delay. The ISO7821LLDWW has different enable propagation delays depending on the logical level present in the input buffer.

This characteristic directly impacts the timing between input and output configuration. For a logical *high* input in the buffer, the output enabling time is 20 ns, and 2.5 μs for a logical *low* input [70].

The timing analysis shown in Fig. 3.15 describes the change of direction between the HV to LV input/outputs. The FPGA handles the HVIO buffer through an internal bidirectional differential IO. The enable signal from the FPGA takes 38 ns to move from HV to LV through the ISO7840FDWW and the discrete inverter gate. For an initial *high* input, the delay time from the enable is 83 ns (Fig. 3.15a). The change of direction starts when the FPGA puts its IO buffer in high impedance (input mode) and rises the HV Enable signal. The output in the LV will be set to zero after 25 ns and before the enable signal reaches the LV domain. This setting implies that there is a time when both enables are set high, causing an *undetermined* value in the HV IO (Fig. 3.15a). Indeed, when the enable signal reaches the LV domain, it takes 20 ns to disable the output buffer; during this time, the LV IO will have an undetermined logical value. After this time, the HVIO buffer is ready to send the first logical value (D0) to the HV domain, with a latency of 25 ns.



(a) High input to high impedance diagram



(b) Low input to high impedance diagram

Figure 3.15: Output to input transition diagram

For an initial *low* value switching, the overall time transition is 2.525 μs due to the slow *enable* propagation delay of the impedance-to-low output on the ISO7821LLDWW. This state leads to a relatively long-lasting *undetermined* value during the switching after the initial 20 ns. The timing diagram is shown in Fig. 3.15b.

3.1.5 Temperature and Pressure Sensors Board

The gain in MPGDs is directly related to the temperature and pressure of the gas chamber. It has been demonstrated that gain stability within a certain error percentage can be maintained over months, even in multistage detectors [50]. One of the requirements of the HVPSS is to provide HV compensation as a function of temperature and pressure. These measurements are obtained by an ADT7420 [72] temperature sensor by Analog Devices and MS5611-01BA03 [73] pressure sensor by TE Connectivity, respectively. Both sensors are mounted into an external PCB designed to be easily inserted into the gaseous detector volume, as shown in Fig. 3.16, and are connected to the SoC through a digital IIC interface.

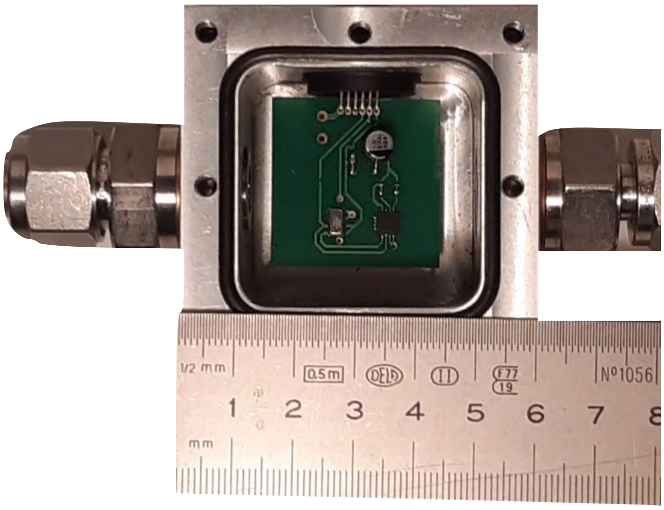


Figure 3.16: Pressure and temperature sensors PCB, hosted in a gas-tight box connected in series with the gas supply line.

The ADT7420 is a high accuracy 16-bit temperature sensor that digitizes temperature with 0.0078 ^{o}C resolution. This sensor is rated for operation between -40 ^{o}C to +150 ^{o}C.

The MS5611 is an integrated digital pressure sensor with ultra-low power 24-bit digital resolution. This sensor has internal factory calibrated coefficients calculated and stored in a 128-bit internal PROM. The MS5611 also has an internal temperature sensor to compensate the pressure measurement. The sensor operation range is 10 to 1200 mbar from -40 to +85 °C.

3.1.6 Decoupled Power Supply

One of the challenges described in Section 3.1.4 is to decouple the HV power domain from the communication layer. The data acquisition and control system (pA, ADC, FPGA) must be placed in the HV power domain, implying that the acquisition electronics must be floating and usually at several kV of the global ground.

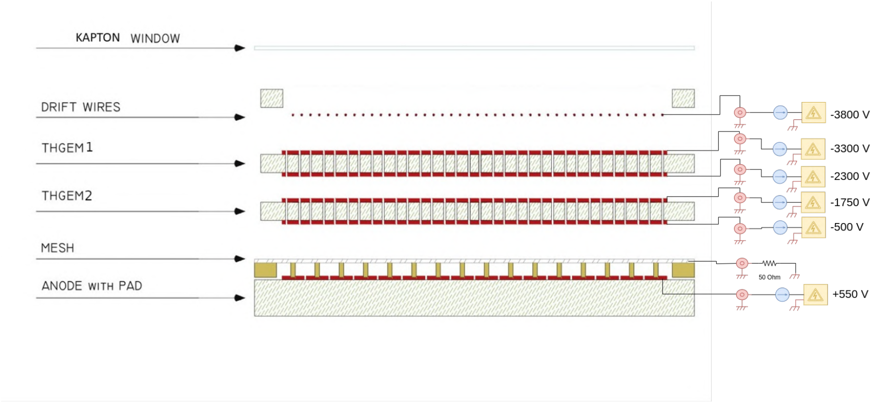
It is important to consider that the MPGD may be polarized using different schemes, as shown in Fig. 3.17. A common ground configuration like the one shown in Fig. 3.17a has the advantage of electrical noise stability and the option of using a single power supply for all channels. One significant disadvantage is the large HV difference between channels and ground. In case of a short circuit to ground failure of a power supply, the remaining potential between electrodes may be too high and produce further electrical discharges.

A cascade configuration like the one shown in Fig. 3.17b has the advantage that it is safer for the detector in case of a damaged HV power supply. However, each HV DC/DC channel needs independent (floating) power supplies, and the floating configuration is more susceptible to electrical noise.

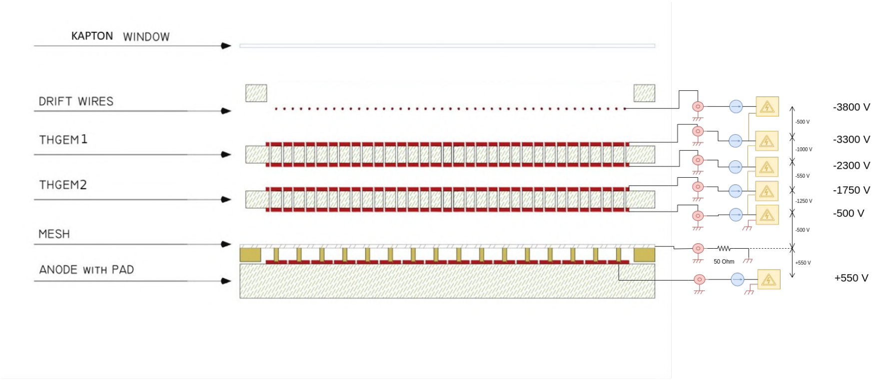
In summary, it is possible to identify three different power domains in each HVPSS channel. One with reference on the absolute ground and two floating ones with their reference (HV Ground and Ctrl System Ground). The different power domains are shown in Fig. 3.18.

Table 3.2 shows the different voltages required to power up the different boards in each power domain. A two stage decoupling was designed to provide power for each HVPSS channel. An isolation transformer does the first stage of decoupling. The selected one was the N-67 Triad Magnetics Transformer, which provides an output voltage of 115 VAC / 1.3 A and up to 2100 V isolation [74]. The second stage is an AC/DC power supply DZ150-7EU to provide the +12 V, and +5 V [75]. The DZ150-7EU is a medical and industrial-grade power supply with active power factor correction, overload, and short circuit protection. This power supply delivers the voltage to the picoammeter board and control system power domain.

Another DZ150-7EU is connected to all HVPSS channels in the Low Voltage (LV) power domain to provide +5 V and +12 V to the network interfaces. Depending on the electrodes polarization configuration, the HV DC/DC Board needs to be connected in one of the configu-



(a) HVPSS Electrode polarization in common ground configuration



(b) HVPSS Electrode polarization in cascade configuration

Figure 3.17: HVPSS Electrode polarization in different configurations

Table 3.2: Voltage required for each board in different power domains.

Power Domain	**Voltage Required**	**Board**
Picoammeter board and Control System Power Domain	+12 V	Picoammeter Board
	+5 V	ADC500 Board, SoC-FPGA
HV Power Domain	+12 V	HV DC/DC Supply Board
LV Power Domain	+5 V	HVIBNI Interposer
	+12 V	Fiber to Ethernet Media Converter

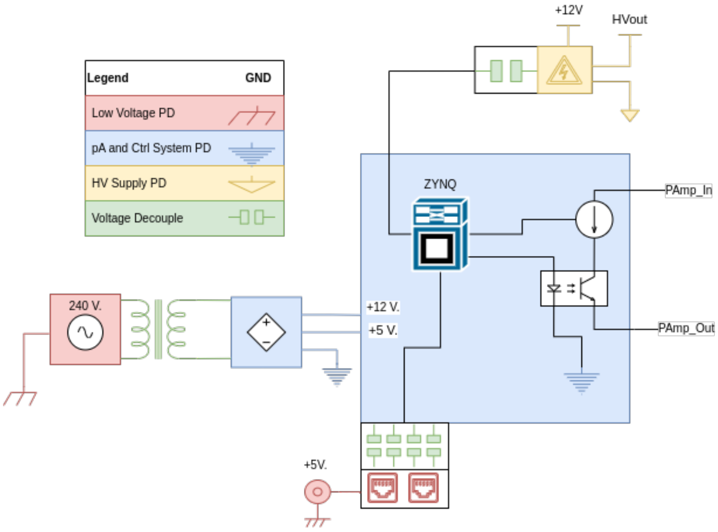
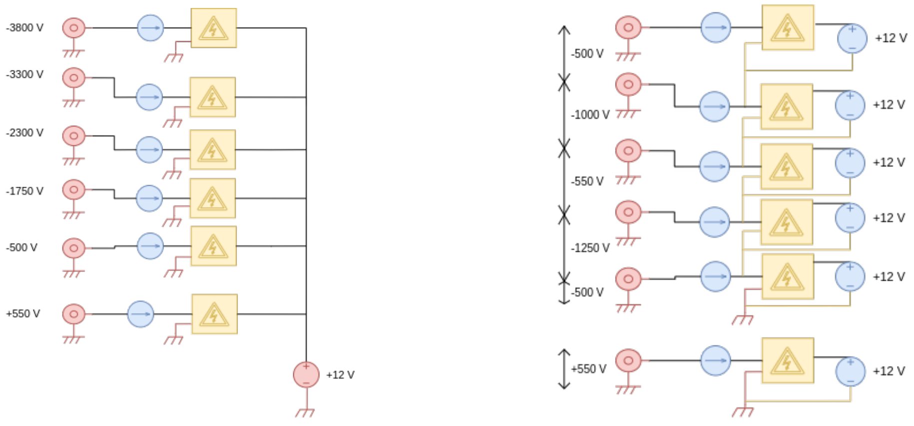


Figure 3.18: Different power domains present in each HVPSS channel

rations shown in Fig. 3.19.



(a) Common Ground

(b) Cascade

Figure 3.19: Power supply connection for HV Power Domain in common ground configuration (3.19a) and cascade configuration (3.19b)

In common ground configuration, all the HV DC/DC supply boards should be connected to the +12 V power supply of the LV power domain as shown in Fig. 3.19a. In cascade configuration, each HV DC/DC supply board needs to be connected to the +12 V corresponding to its corresponding *pA and Ctrl System PD* as shown in Fig. 3.19b.

3.1.7 SoC-FPGA Board

The core of the system is based on a Xilinx ZYNQ SoC-FPGA device. This device combines a dual-core ARM Cortex A9 microprocessor with an FPGA fabric in a single chip [76]. This device was chosen considering the requirements for the HVPSS established at the beginning of this chapter 3. The time critical tasks such as high-speed data acquisition, timestamping, and time synchronization are done in the FPGA. Non-time critical tasks such as slow-control and Ethernet interconnection are done in the microprocessor. These tasks are explained in detail in the chapter 4.

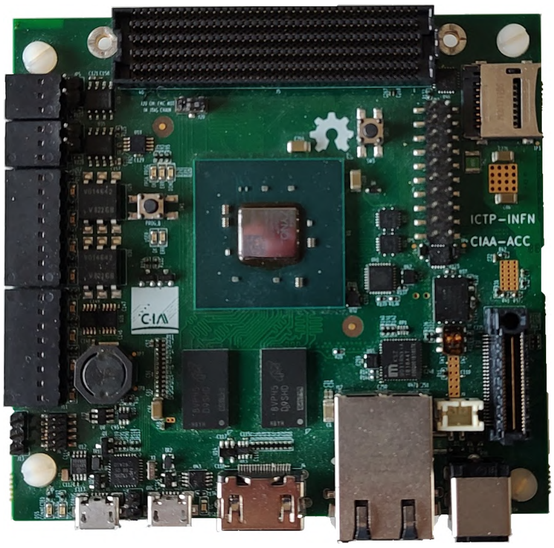


Figure 3.20: CIAA-ACC SoC-FPGA Board

The first prototype of a HVPSS channel was built in a Zedboard commercial carrier board using a Zynq-7020 (XC7Z020 [77]). The board contains 512 MB of DDR3 memory, 10/100/1000 Ethernet, FMC-LPC connector. The SoC has a Dual-Core ARM Cortex-A9 MPCore with clock frequency up to 866 MHz, 256 KB On-Chip Memory. The FPGA has 85K logical cells, 53200 Look-Up-Tables (LUTs), 106400 Flip-Flops, 220 Digital Signal Processor (DSP) slices, and 4.9 Mb of total block RAM.

The first stage of development proved the correct choice of the SoC-FPGA architecture. The need for an industrial level board with a smaller physical size leads to adopting a custom open-hardware carrier. This board was designed by the Argentinian National Institute of Industrial Technology (INTI). The adopted board, namely CIAA-ACC, is a high pin count (HPC) FMC carrier (ANSI VITA 57.1 standard) based on a Zynq-7030 [78]. The CIAA-ACC SoC-FPGA board is shown in Fig. 3.20.

3.2 Summary

The special requirements for the HVPSS channels lead to the development of an *ad-hoc* hardware solution, including the study of various technologies and devices. Several components were investigated and characterized to find out whether they fit the requirements of the design. A modular approach simplifies the system's maintenance and upgrades with reduced effort.

A picture of a HVPSS channel with its respective hardware boards is shown in Fig. 3.21.

The final system includes seven hardware boards: the HV DC/DC supply board provides a low noise HV DC output from 0 to -4 kV with 16-bit resolution in control and 18-bit in the monitoring interface with a HV isolation interface for the SPI bus. The picoammeter board provides the low current measurements (with picoamperes of precision) in two different ranges and digital offset control of a HV power domain. The high-speed ADC board captures fast transient events with 2 ns time resolution. The HVIBNI designed in the interposer board provides a 100 Mhz network interface for communication among different HVPSS channels in different HV power domains. The temperature and pressure sensors provide a 24-bit resolution readout needed for automatic compensation in the HVPSS baseline to keep the gain of the detector stable. A decoupled power supply system provides power to the entire HVPSS channel with its different power domains allowing flexible configuration according to the system needs. Finally, the CIAA-ACC board housing a Zynq 7030 SoC-FPGA provides control of every component of the system. Several prototypes and versions of each board were built to reach this point. Many of them were tested in laboratory conditions at ICTP, INFN, and RD51; and in test beam conditions at CERN (described in Chapter 6). Having the proper hardware is half the way to meeting the requirements of the HVPSS. The high-speed resolution needs a control system capable of handling these hardware blocks. The firmware development and control software is discussed in Chapter 4.

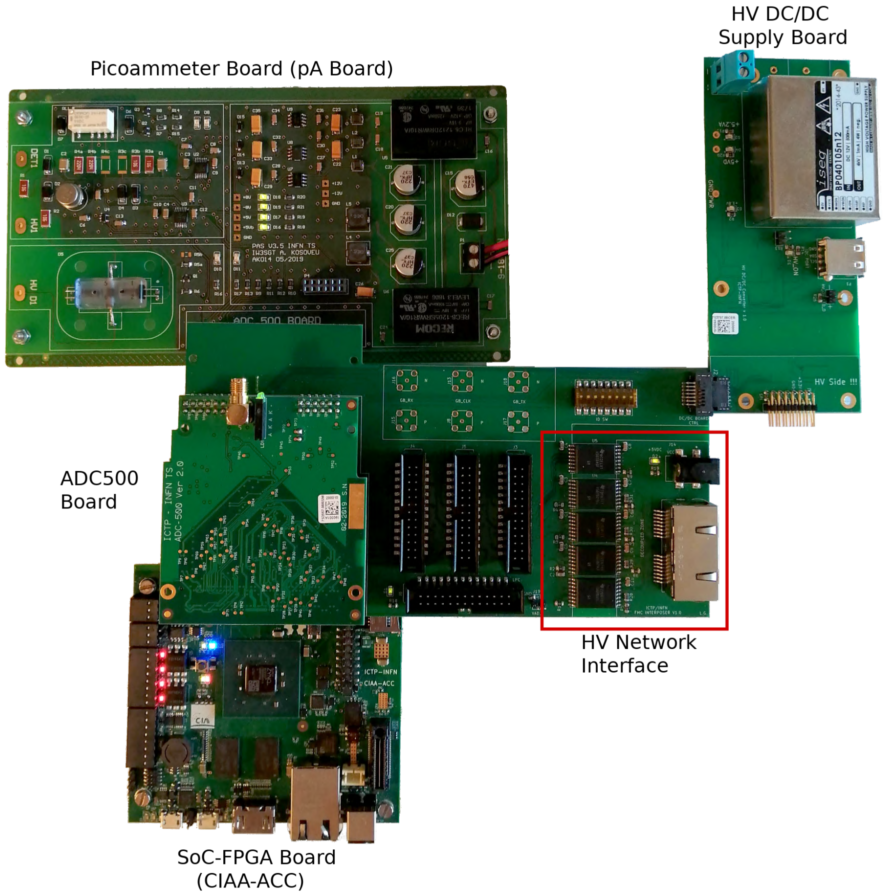


Figure 3.21: HVPSS channel with its corresponding hardware boards

Chapter 4

Firmware and Control Software Development and Implementation

The previous chapter described the hardware requirements leading to the selection of a SoC-FPGA as the system's controller. As described in 3.1.7 the combination of an FPGA to perform time-critical tasks; with the microprocessor (μP) for executing sequential tasks, this technology is ideal for the development of advanced scientific instrumentation. The SoC-FPGA also opens the possibility for reconfigurable instrumentation for custom applications and upgrades ad-hoc to the needs of the detectors.

Full-stack development of SoC-FPGA applications includes core FPGA design, μP software and drivers, and user control software. Devices like the Zynq family provide a huge amount of reconfigurable logic and computational resources for implementing complex systems. A modular Open-Source Firmware Architecture (OSFA) for remote control shown in Fig. 4.1 was adopted to simplify the design tree complexity and to ensure the portability for future upgrades [79].

This development framework acts like a pre-built simple interface between the user and the design cores on the FPGA with minimum configuration in the μP. However, this architecture also leaves room for application-specific software to perform tasks more suitable for a μP. An implementation of this framework has been successfully tested in different contexts, including remote laboratories for e-learning with applications on nuclear and scientific instrumentation [80].

Now that the base architecture has been defined, the best way of describing the firmware

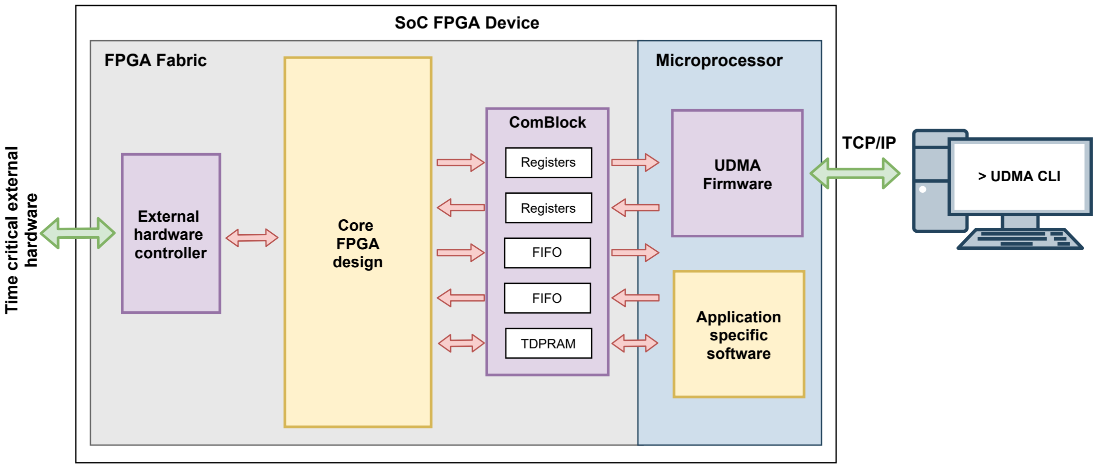


Figure 4.1: Block diagram with the main components of the OSFA implemented in SoC-FPGA. The purple boxes provide common services, and the yellow boxes are the user's free design and programming areas.

components and design is by splitting this chapter into three main sections:

- The FPGA firmware design (Section 4.1).
- The μP firmware and application-specific software (Section 4.2).
- The PC software interface and remote communication (Section 4.3).

4.1 The FPGA Firmware Design

The FPGA manages a 500 MHz data stream and detects fast transient phenomena within 2 ns of time resolution. These events are sampled and logged for further studies. The FPGA also handles the time synchronization in all the HVPSS channels within 20 ns of error among channels.

Fig. 4.2 shows the block diagram of the logical cores developed inside the FPGA. Blocks shown in purple are the external hardware-interface cores tasked to communicate and retrieve data from the external hardware boards through different data busses (red arrows). Red blocks are the fast transient manager tasked with detecting and log high-speed events. Green blocks represent data processing cores and diagnostic tools used for signal conditioning to improve

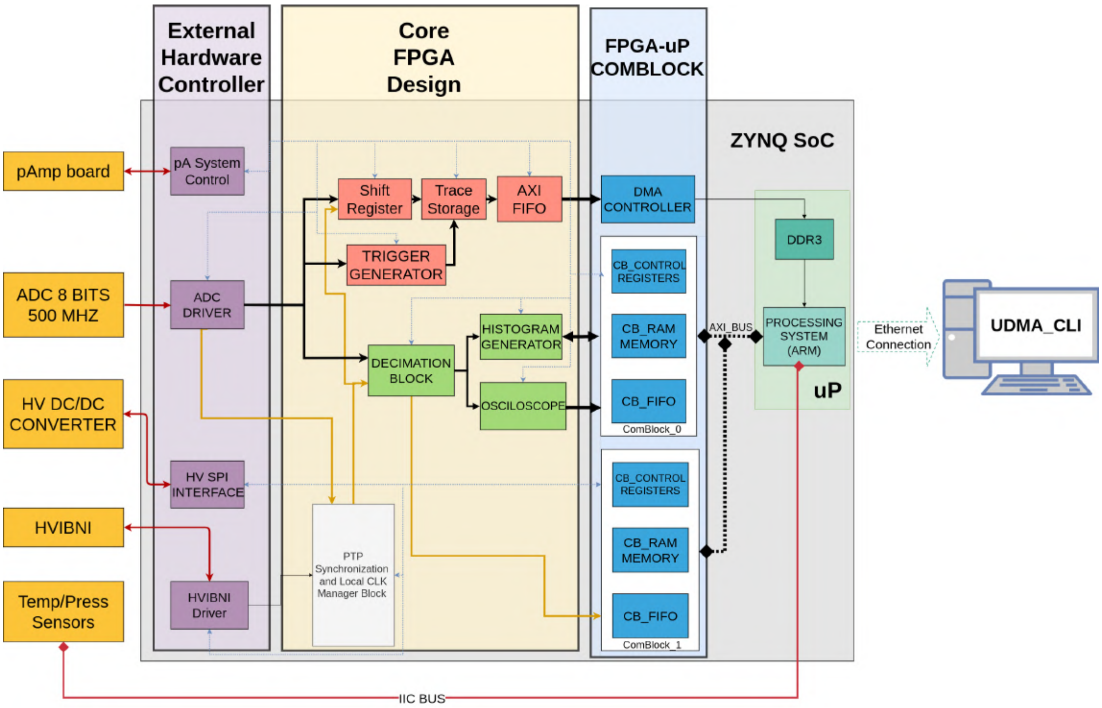


Figure 4.2: Block diagram of the RTL blocks that constitute the FPGA firmware for the HVPSS channel.

and log data coming from the sensors. The white block core handles time synchronization and local clock to provide an accurate time reference in all data taking and channels. Blue blocks are the FPGA-μP interface cores used to transfer data to and from the μP. Further details of each block function and design are described in the following subsections.

The described blocks were designed in a register-transfer-level (RTL) abstraction level described in VHDL. The Integrated Design Environment (IDE) tool was Vivado 2019.1. The system clock running in the FPGA is 250 MHz, providing a 500 MHz clock to the high-speed ADC. The resource utilization of the entire system on the Zynq-7030 is shown in Fig. 4.3.

The following subsections describe the working principle of the different RTL blocks designed for the HVPSS. From here on, in this chapter, the names of the blocks will be written in a bold-italic font (e.g., ***Block_name***), and the names of the signals and registers will be written in italic (e.g., *Register*).

Resource	Utilization	Available	Utilization %
LUT	12911	78600	16.43
LUTRAM	1800	26600	6.77
FF	18198	157200	11.58
BRAM	69.50	265	26.23
IO	85	250	34.00
BUFG	9	32	28.13
MMCM	1	5	20.00

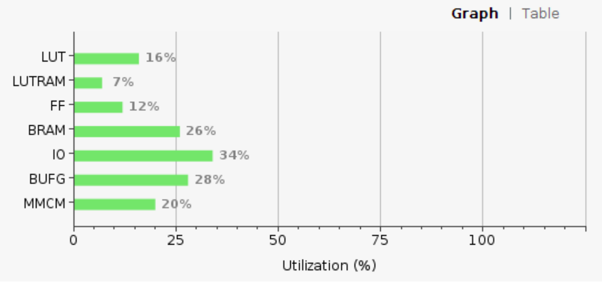


Figure 4.3: Zynq-7030 HVPSS channel resources utilization

4.1.1 Hardware Interface Blocks

These blocks drive all the different hardware boards mentioned in Chapter 3. The following interfaces communicate with the different elements of the HVPSS channel:

- Low voltage CMOS GPIO.
- Serial Peripheral Interfaces (SPI)
- 16 LVDS input data signal.
- 4 LVDS input/output data buffer.

ADC Driver Block

The ***ADC_driver*** block is designed to control the high-speed ADC board (section 3.1.3). It provides a 500 MHz LVDS clock output to the ADC board. It receives two consecutive 8 bits samples in a parallel data bus of 16 bits LVDS synchronous with a 250 MHz clock from the ADC. A 64 bits sample counter is implemented in the driver, which increases with the sample clock allowing to keep a time reference in case the data acquisition stops in the other blocks of the system. The counter is also used to achieve the 2 ns timestamp by analyzing consecutive samples. This implementation is described in Section 4.1.3.

The ADC driver block has two readout outputs:

1. **RAW data output:** It comprises the direct 16 bits data samples (MSB and LSB) output, and the 64 bits counter synchronized with the 250 MHz data sampling clock.

2. **Clock Domain Crossing (CDC) output:** The output is a 32 bits bus (DOUT) and a data valid (DVALID), both synchronized with the system clock. The bus combines the 16 bits data from the ADC and the least significant 16 bits of the counter. The cross-domain clocking is based on a FIFO circuit to pass the data to different clock domains.

The difference between the RAW counter and CDC counter is used to calculate the latency of the readout within ≈ 262 μs.

Two registers are implemented in the driver, one for the status flags and the other for the configuration. These configuration flags are detailed in Table 4.1. Further details are found in the core specific git [81].

Table 4.1: Input/Output registers for the ADC500 board.

Pin	**Register bit**	**Description**
x_to_adc_cal_fmc	Ctrl_reg_in(0)	Calibration Cycle High initiate Calibration
x_to_adc_caldly_nscs_fmc	Ctrl_reg_in(1)	Calibration Delay and Serial Interface Chip Select.
x_to_adc_fsr_ece_fmc	Ctrl_reg_in(2)	Full Scale Range Select and Extended Control Enable.
x_to_adc_outv_slck_fmc	Ctrl_reg_in(3)	Output Voltage Amplitude and Serial Interface Clock.
x_to_adc_outedge_ddr_sdata_fmc	Ctrl_reg_in(4)	DCLK Edge Select, Double Data Rate Enable and Serial Data Input.
x_to_adc_dclk_rst_fmc	Ctrl_reg_in(5)	DCLK Reset.
x_to_adc_pd_fmc	Ctrl_reg_in(6)	Power Down
x_to_adc_led_0	Ctrl_reg_in(7)	LED 0
x_to_adc_led_1	Ctrl_reg_in(8)	LED 1
x_to_adc_reset_counter	Ctrl_reg_in(9)	Resets internal counter when this bit is asserted. Free-running counter otherwise.
	Ctrl_reg_in(10..31)	Reserved

Pin	**Register bit**	**Description**
x_from_adc_calrun_fmc	Ctrl_reg_out(0)	Calibration Running indication.
x_from_adc_or(0)	Ctrl_reg_out(1)	Out Of Range output
(others=>’0’)	Ctrl_reg_out(31 downto 2)	Reserved

The Picoammeter System Control and the HV SPI Control

The Picoammeter System Control (***pAS_Ctrl***) and the HV SPI control (***HV_CTRL***) blocks provide an SPI communication driver to the Picoammeter board (section 3.1.2) and the HV DC/DC Supply board (section 3.1.1) respectively. The main reason that both blocks are separated is to add extra security measures (*HV_nOn*) in the ***HV_CTRL*** to prevent accidental changes in the HV.

The SPI controller is based on a *spi_master.vhd* VHDL code from digikey TechForum [82]. This code is modified to meet the design-specific needs. It is instantiated into the ***PAS_Ctrl*** and ***HV_CTRL*** blocks to provide an interface with the following registers: configuration, data output, data input, and enable transmission (SPI_CFG, SPI_TX, SPI_RX, and enable_tx respectively). The configuration register allows setting transmission frequency, target address, phase, polarity, and continuous transmission mode. The specific bits are described in Table 4.2.

Table 4.2: SPI Configuration Register

SPI Configuration Register	Name	Description
SPI_CFG[31..24]	CLK_DIV	Clock Divider
SPI_CFG[23..16]	ADDR	Target Address
SPI_CFG[2]	cont	Continous mode high= continuous low= single
SPI_CFG[1]	cpha	phase
SPI_CFG[0]	pol	polarity

A timing diagram of the effects of the *SPI_CFG* register is shown in Fig. 4.4.

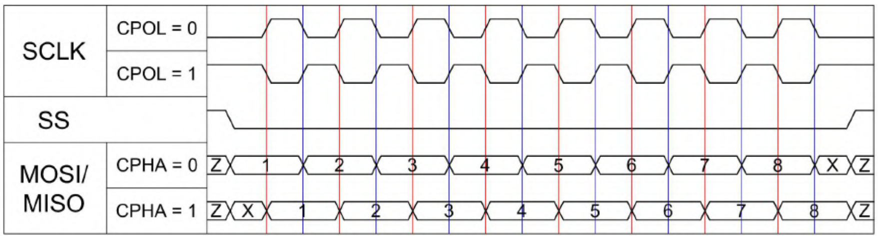


Figure 4.4: SPI Master timing diagram (source: Digikey TechForum [82])

The HVIBNI Driver

The final hardware-interface block described in this section is the High Voltage Isolated Bidirectional Network Interface (HVIBNI) Driver to control the hardware interface described in Section 3.1.4. This driver sets and controls the flow of four bidirectional LVDS signal pairs. The core uses the series 7 primitive Bi-Directional Differential Buffer with Digital Controlled Impedance (DCI) Enable/Disable and Input Disable (IOBUFDS_DCIEN) to connect the internal logic to an external bidirectional pin [83]. Fig. 4.5 shows the different configuration ports available for this primitive.

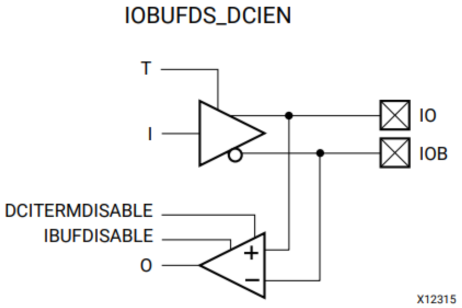


Figure 4.5: Primitive: Bi-Directional Differential Buffer with DCI Enable/Disable and Input Disable [83].

This primitive has an input path disable (IBUFDISABLE) flag that allows disconnecting the output to the FPGA from the incoming signal. During the buffer transition from input to output, the IBUFDISABLE flag and the high impedance (T) flag of the input signal coming from the FPGA are enabled to keep a clean transition of direction in the HVIBNI (Fig. 3.15, Section 3.1.4) without, affecting the data flow inside the FPGA.

4.1.2 PTP Synchronization and Local Time Manager Block

This block is in charge of handling and distributing the local time as well as to synchronize with the other HVPSS channels to keep a coherent timescale among the systems. The local time is taken from the ADC sample counter. The synchronization among HVPSS channels is done by selecting one as the master clock as a reference for the other channels. A modified version of the IEEE-1588 does the synchronization between master and slave-2019 Precise Time Protocol (PTP) standard [84]. The main difference from the standard is that the current implementation is simplified for a minimum synchronization in a line topology interconnection with a reduced header indicating only the type of message, the slave address, and the timestamp, with more advanced features left for future implementations. However, the concept of time synchronization is preserved. Figure 4.6 shows the principle of operation of the implemented protocol.

If we call Δ_n the time difference between the master clock time (MT) and the N slave clock time (SNT), the relation between both can be defined with the following equation:

$$MT = SNT + \Delta_n. \tag{4.1}$$

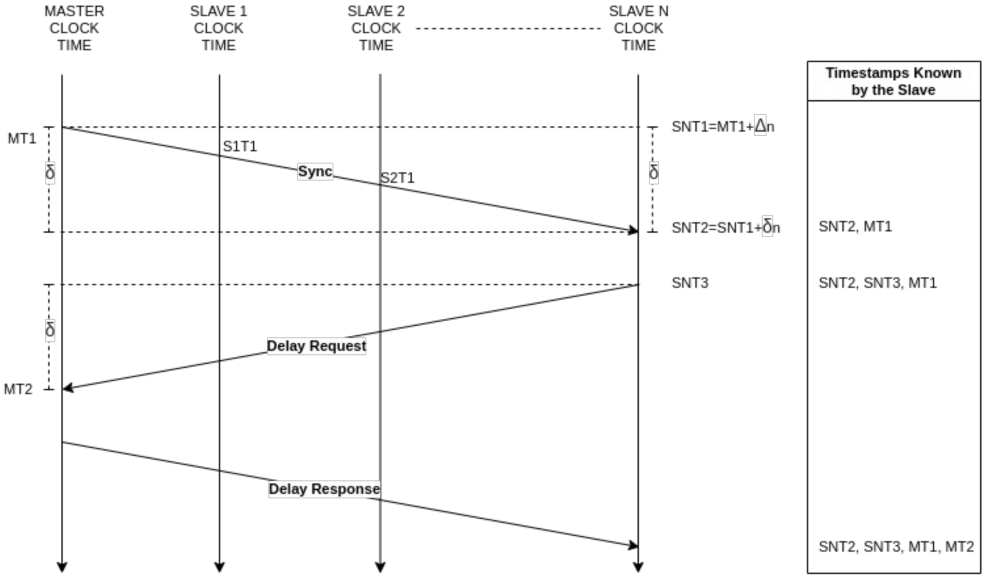


Figure 4.6: Simplified PTP principle of operation for multiple slaves.

To calculate this delay, the procedure is described below.

1. The master sends a *Sync* signal, its address, and the timestamp MT_1 to the slave N in a single package. All the slaves take a timestamp SNT_2 as soon as the *Sync* signal arrives, which is kept until the address is validated. The MT_1 time is then stored in the intended slave for synchronization;
2. In a time SNT_3, the slave sends a *Delay Request* to the master. The master takes a timestamp MT_2 as soon as the request is received;
3. The master sends the timestamp MT_2 to the slave with a header *Delay Response*, opening the communication channel;
4. The slave calculates the time correction using the obtained information.

Assuming that the delay of the channel δ_n is symmetrical for transmission and reception, we can deduce the equations to calculate the time correction Δ_n using as reference Figure 4.6. The base equations are the following:

$$SNT_1 = MT_1 + \Delta_n; \tag{4.2}$$

$$SNT_2 = SNT_1 + \delta_n; \tag{4.3}$$

$$MT_2 - MT_1 - 2\delta_n = SNT_3 - SNT_2. \tag{4.4}$$

By simplifying these equations we obtain the following results:

$$\delta_n = \frac{SNT_2 - SNT_3 + MT_2 - MT_1}{2}; \tag{4.5}$$

$$\Delta_n = \frac{SNT_2 + SNT_3 - MT_1 - MT_2}{2}. \tag{4.6}$$

With these equations and the relationship described in Eq. 4.1, it is possible to synchronize the clocks to the master clock.

The synchronization routine is performed by the master, sending the *Sync* signal, one by one, to all the slaves in the system. By default, all the modules are set up in a slave configuration with the exception of the address 0, which is reserved for the master. These configurations can be overridden by register. The initial configuration of the four HVIBNI buffers depends on wether the module is set up as a master or slave. The master has a static input/output configuration with two buffers configured as outputs and two as inputs. The slaves have all buffers initially configured as input; this will change after the address sent by the master is verified, changing the configuration of one buffer to the output. This allows full duplex communication between master and slave until the channel is released, changing back the slave buffers to input.

Universal Asynchronous Receiver / Transmitter (UART) protocol was selected to communicate between channels. This protocol was chosen for its asynchronous nature, which allows one to read and write independently the delays that the buffers may cause. The *Start Bit* falling edge is ideal to timestamp the SNT_2 during the *Sync* message and the MT_2 during the *Delay Request*. By implementing it in the FPGA, the baud rate can be as high as the HVIBNI allows it (100 MHz) and the number of bits transmitted as long as the message requires, as shown in Fig. 4.7. Even though the maximum transmission frequency is 100 MHz, to reduce the probability of bit slipping during the UART transmission, the frequency was limited to 80 MHz to guarantee the integrity of the package.

The whole process is handled by a RTL block implemented in the FPGA. This block can be programmed in a master or slave configuration selected with the *MSFLAG* port. A detailed

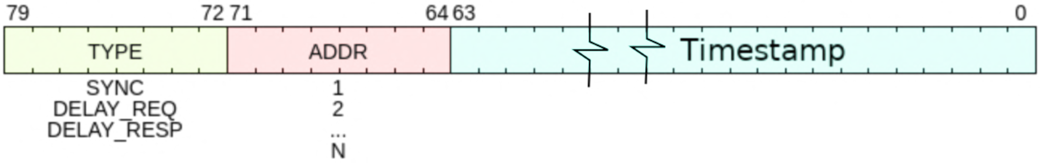


Figure 4.7: Type, Address (ADDR) and Timestamp packed for PTP transmission throug the HVIBNI.

description of the state machine implemented in VHDL is presented in Fig. 4.8. At power up or enable, the block will read the $MSFLAG$ value to determine the master or slave configuration.

On "Master" configuration, the block will be on an idle state waiting for the *Sync Start* flag rise to high. When this happens, a *Sync* message is sent to the address, $ADDR$. The timestamp MT_1 is stored at the falling edge of the start bit from the UART and queued to the end of the package during the transmission in the state *TX_Sync*. After finishing the transmission of the package, the state changes to *RX_Delay_Req*. In this state, the master waits for the delay request (*Delay_Req*) from the slave. In parallel, a timeout clock starts running in case the slave does not answer on time. If this condition is reached, the transaction is ended and the state machine goes back to idle. If the *Delay_Req* signal is received, the timestamp MT_2 is stored until the address is verified. After ending the transmission of the delay request, the process changes to the state *TX_Delay_resp* where the timestamp is packed and sent (*Delay_Resp*), ending the process and going back to idle.

On "Slave" configuration, the block is idle waiting for the *Sync* signal to be received, and when the start bit arrives, the SNT_2 timestamp is stored and kept until the address is received and verified in the state *RX_Sync*. In the event that the address does not match, the timestamp is dropped and the state goes back to Slave idle. If the address matches, the MT_1 timestamp is received and stored. In the state *TX_Delay_Req*, the slave sends a *Delay_Req* package, thereby capturing the SNT_3 timestamp as soon as the start bit of the UART transmission begins queuing it at the end of the package. The next state *RX_Delay_Resp* waits for the *Delay_Resp* package to read the MT_2 timestamp, completing the information needed to do the correction.

On master configuration, the corrected time ($CTIME$) in the master is the same as the local time and will remain unchanged during the whole process. On slave configuration, the correction happens as soon as the *RX_Delay_Resp* state is finished, raising a correction ready,

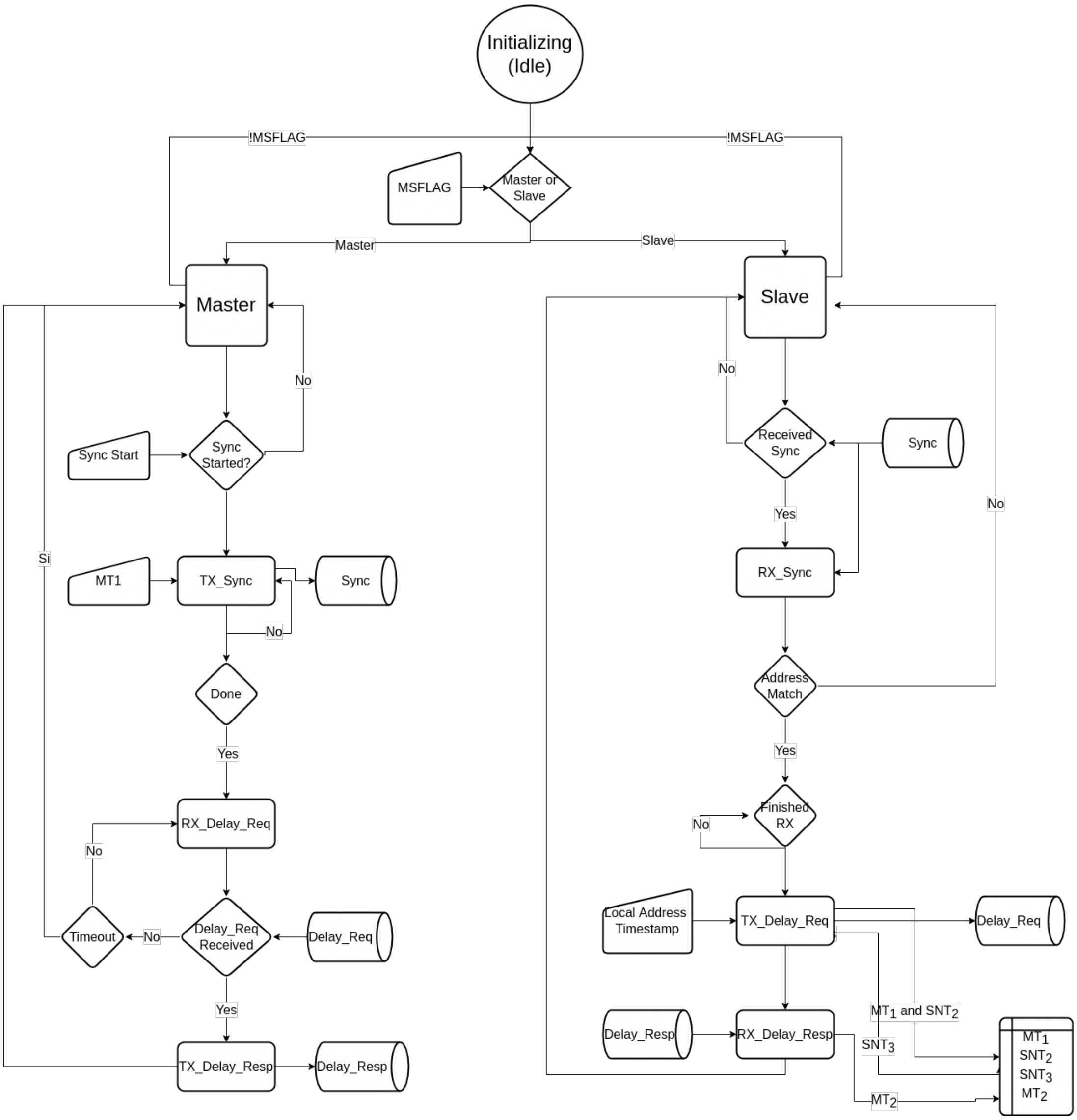


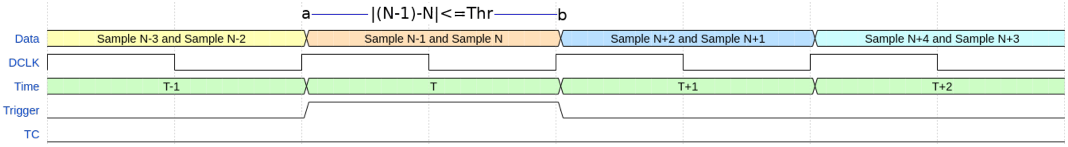
Figure 4.8: Simple PTP state diagram.

CTRDY, flag high. By default *CTRDY* is set on low until successful synchronization.

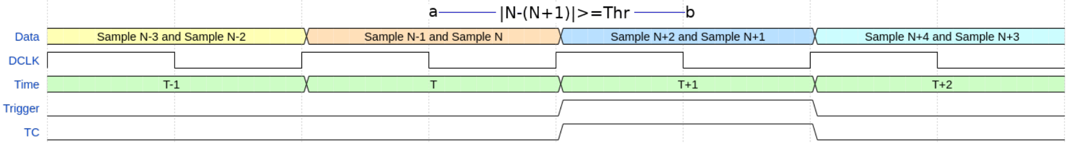
4.1.3 Fast Transient Capture Blocks

These blocks task is to detect fast transient events, timestamp them, store several samples around the event and pack them for transmission. The data input is stored in a circular buffer based on a ***shift register*** block and controlled by trace storage before queuing it in a FIFO to be transmitted to the μP. A description of the blocks is detailed below.

The ***Trigger Generator*** block scans the input signal and rise a flag when a fast transient event is detected. This block measures the difference of consecutive samples and compare it with a fix threshold as shown in Fig. 4.9a. A time correction (TC) flag is raised (Fig. 4.9b) if the trigger condition happens between two different packages. A TC flag means that the recorded time needs a 2 ns time correction due to the event happening in the middle of a data clock (DCLCK) cycle.



(a) Trigger event generation in two consecutive samples from the same package.



(b) Trigger event generation in two consecutive samples from different package.

Figure 4.9: Trigger generation conditions.

The ***Trace_Storage_Manager*** task is to prepare N number of samples before and after the trigger signal arrives. It is done by handling a shift register as a circular buffer; and enabling the number of samples to be written into a FIFO to complete the trace. The data-trace contains the clock information coming from the timing management system (Section 4.1.2). The package format to be transmitted is shown in Fig. 4.10. This format foresees a header including information on the number of samples before and after a trigger, a correlative event number and a start-of-header character. The timestamp is stored at the moment of the trigger as a global reference. Each sample contains the less significant 16 bits of its corresponding timestamp. The package ends with a line including the information on correlative event number as redundancy and a time correction (TC) flag from the trigger generation block.

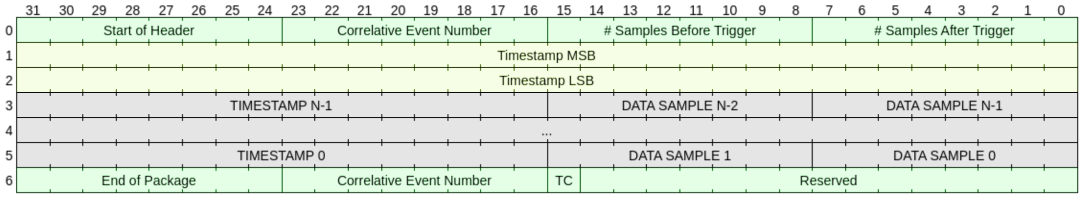


Figure 4.10: Fast transient package format for transmission.

4.1.4 Data Processing Blocks

Three data processing blocks where implemented, a decimation block, an oscilloscope block and a histogram block. These blocks process the picoammeter data and provides sampling and analysis tools of the current measurements.

Oversampling and Decimation

The minimum design requirement is to provide current measurements with a resolution of 10 pA at a sampling rate of approximately 100 kHz. As mentioned in Section 3.1.2 in the trans-impedance Eq. 3.4, the voltage output depends on the feedback resistor. With a 10 $M\Omega$ with an input range of the ADC of 320 mV, the initial current resolution for 8-bit sampling is 125 pA with a range of $\approx$ 30.6 nA. Increasing the feedback resistor leads to an increase in the noise and destabilizing effect with the internal capacitance of the amplifier [85].

One solution is to implement an oversampling method on the FPGA to increase the virtual resolution of the sampled signal. Using this method is possible to increase the effective number of sampling bits n_b by sampling N number of samples according to eq. 4.7. Many systems employ oversampling decimation to improve anti-aliasing and to reduce noise in digital systems [86], [87].

$$n_b = \left(8 + \frac{1}{2}\log_2 N\right) \tag{4.7}$$

The working principle of decimation by oversampling is to process a signal to a sampling frequency significantly higher than the Nyquist rate. These extra samples increase the dynamic range of the ADC by a factor of N because there are N times as many possible values for the sum. Assuming the noise contains sufficient uncorrelated components to be approximated as white noise, the quantization noise power (σ^2) is defined by eq. 4.8 where the nominal resolution for the ADC of n bits with a range V_r is $\Delta = V_r/2^n$.

$$\sigma^2 = \frac{\Delta^2}{12} = \frac{V_r^2}{12}\,2^{-2n} \tag{4.8}$$

Therefore, the power spectral density for the ADC sampling frequency range f_s is:

$$P(f) = \frac{\sigma^2}{f_s} \tag{4.9}$$

After the decimation process is applied, the oversampling frequency (f_N) is reduced in a factor of N becoming:

$$f_N = \frac{f_s}{N} \tag{4.10}$$

To prevent aliasing, the new sampling frequency must meet the Nyquist sampling theorem. Therefore, the maximum frequency (f_{max}) such that no aliasing noise is introduced must be:

$$f_{max} < \frac{f_s}{2N} \tag{4.11}$$

This means that only a portion of quantization noise power in the range from $\pm f_{max}$ is kept. This changes the quantization noise power after applying a decimation of N by the following expression:

$$\sigma_N^2 = \int_{-f_{max}}^{f_{max}} P(f)df = \frac{\sigma^2}{f_s} f\Big|_{-f_{max}}^{f_{max}} = \left(\frac{2f_{max}}{f_s}\right)\sigma^2 = \left(\frac{2f_{max}}{f_s}\right)\frac{V_r^2}{12}\,2^{-2n} \tag{4.12}$$

Eq. 4.12 can be expressed in terms of 4.8 for an n_b bits ADC with a sampling frequency f_{max}

$$2^{-2n_b} = \left(\frac{2f_{max}}{f_s}\right) 2^{-2n} \tag{4.13}$$

which leads to the following equations:

$$n_b = n + \frac{1}{2}\log_2\left(\frac{f_s}{2f_{max}}\right) \tag{4.14}$$

$$f_s = 2\ f_{max}\ 2^{2(n_b-n)} \tag{4.15}$$

Where Eq. 4.14 is the general expression of Eq. 4.7 for an 8-bit ADC. And Eq. 4.15 is the minimum sampling rate to keep the Nyquist frequency. The signal-to-noise ratio (SNR) also increases because integrating uncorrelated noise increases its amplitude by $\sqrt{N}$, while the signal contribution increases by N. The SNR will only improve if the noise can be approximated to white noise. The input signal needs to change randomly with each variation equally probable in an amplitude range comparable to the nominal resolution Δ of the ADC for this to be valid. If the overall noise is not stationary, then the oversampling and averaging may not be effective [87].

The decimation block implemented for this project integrates the signal over N number of samples in free running mode indicating with a *data_valid* flag that the value is ready for reading. The decimation factor and a reset signal are set by register. The maximum number of input (n) and output (n_b) bits to be processed are set up as a generic in the RTL block before synthesis. Therefore, the maximum decimation possible for the block is defined by Eq. 4.16. The only tested limitations of the number of bits are the resources available on the FPGA.

$$N_{Max} = 2^{2(n_b - n)} \tag{4.16}$$

Oscilloscope and Histogram Generator

The oscilloscope block provides a direct readout of the decimated signal. This block captures a fixed number of samples in a circular buffer until a trigger condition is met. The core transfer the buffered data to a FIFO and counts a number of samples after the trigger to finish the trace. The block has four trigger modes: rising edge, falling edge, auto-trigger, and external trigger.

The oscilloscope is configured by four registers: samples before trigger (SBT), samples after trigger (SAT), trigger level (*Trig_level*), and oscilloscope configuration (*Oscilo_cfg*) register. The last one handles the trigger edge and sets the configuration of the previous registers into the block.

As mentioned in Section 4.1.4, for a proper behavior of the the decimation block it is important to have noise with uniform probability distribution. A practical mean for determining if the noise characteristics is by analyzing the data trough a histogram. The ***histogram generator*** block gives an approximation of the probability density function (PDF) of the signal.

An ideal baseline should have a Gaussian-like PDF. However, the floating nature of the system makes it susceptible to environmental noise. The shape of the histogram gives us an idea of possible artifacts like the one shown in Fig. 4.11.

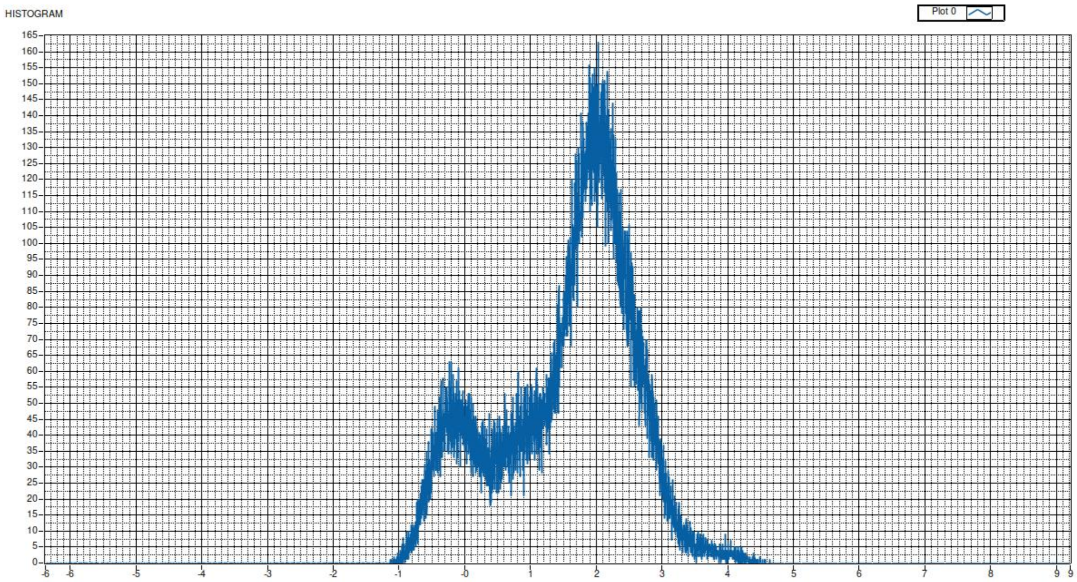


Figure 4.11: Effects of periodic noise in the histogram of the picoammeter.

The ***Histogram_Generator*** block is configured by two registers. The N register sets the number of samples to be stored in the histogram. The control register (*CTRL_REG*) allows to reset and to enable/disable the counter. The histogram is generated in an external RAM memory which is handled by the block.

4.1.5 FPGA-μP Communication Block

The Zynq system provides several tools to interface the FPGA with the μP. The most common is called Advanced eXtensible Interface (AXI) wich is part of the Advanced Microcontroller Bus Architecture (AMBA) [88]. This open protocol has different variants such as AXI FULL (AXIF), AXI LITE (AXIL), and AXI STREAM (AXIS) and many optional signals making it a versatile bus for different applications. This versatility comes with the problem of an increased learning curve that may be overwhelming for some users.

The SoC-FPGA architecture shown at the beginning of this chapter (Fig. 4.1) proposes the use of a communication block (ComBlock) to transfer data between the FPGA and the μP. The ComBlock is the result of a collaboration between the ICTP Multidisciplinary Laboratory (MLAB-ICTP) and the FPGA division of Micro and Nanotechnology of the National Institute of Industrial Technology (INTI, Argentina) [89]. The ComBlock is designed in VHDL to make it portable. The ComBlock was created to provide known interfaces to avoid the complexity of handling several AXI Interfaces for each VHDL block designed by the user [90].

The ComBlock interfaces are:

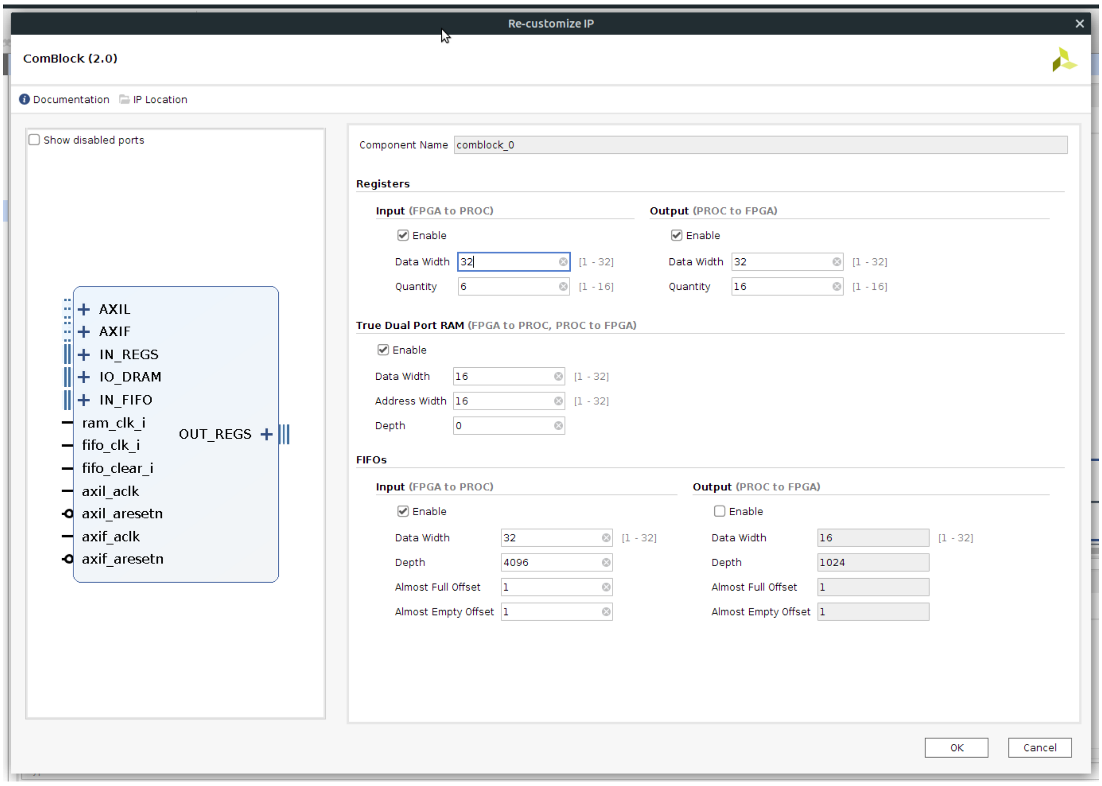
- 0 to 16 input and output registers
- input and output FIFOs
- True dual port RAM (TDPRAM) with share access from the FPGA and the μP.

The ComBlock communication with the μP is through an AXIL interface for the registers and FIFOs, and through AXIF for the TDPRAM. These interfaces are depicted in the IP configuration wizard shown in Fig. 4.12. The current HVPSS channel design uses two ComBlock to access all the FPGA blocks described in Fig. 4.2 from the μP.

The CORE-ComBlock project is available in a git repository is licensed under the BSD 3-clause [89]. A C driver compatible with bare metal and FreeRTOS codes is provided with the ComBlock to be used in the μP. The register map and resources specific details are available in *The ComBlock User Guide* available also in the git.

Direct Memory Access (DMA) block for priority communication

Higher priority data such as the information of the electrical discharges (Section 4.1.3) are stored in memory using a DMA interface. This Xilinx core provides high-bandwidth direct memory access with optional scatter gather capabilities. The selection of this block is to provide to the μP the information of the electrical discharges in a privileged way. The transmission from the FPGA to the memory is initiated by the μP by pooling or by interruption.



Component Name comblock_0

Registers

Input (FPGA to PROC)
☑ Enable
Data Width 32 [1 - 32]
Quantity 6 [1 - 16]

Output (PROC to FPGA)
☑ Enable
Data Width 32 [1 - 32]
Quantity 16 [1 - 16]

True Dual Port RAM (FPGA to PROC, PROC to FPGA)
☑ Enable
Data Width 16 [1 - 32]
Address Width 16 [1 - 32]
Depth 0

FIFOs

Input (FPGA to PROC)
☑ Enable
Data Width 32 [1 - 32]
Depth 4096
Almost Full Offset 1
Almost Empty Offset 1

Output (PROC to FPGA)
☐ Enable
Data Width 16 [1 - 32]
Depth 1024
Almost Full Offset 1
Almost Empty Offset 1

Figure 4.12: ComBlock customize IP wizard showing the configuration options available.

4.2 UDMA Firmware and Application Specific Software in the μP

The embedded μP in the SoC-FPGA runs a real-time operating system (FreeRTOS) to grant predictable timing responses and to facilitate the executions of concurrent tasks including data transmission through the TCP/IP protocol. The μP retrieves the data from the ComBlock and temporary stores these data in an external RAM. A different task of the μP retrieves these data and sends them to the PC as a special data package through the Ethernet port. The communication between the ComBlock and a control PC is handled by the *Universal Direct Memory Access* (UDMA) firmware running in the μP.

UDMA Commands for ComBlock Interface

The transfer of data from one place to another of the global system is described by a special UDMA instruction [79]. A generic UDMA instruction can be expressed as follows:

$$UDMA < src\_addr >< dst\_addr >< src\_inc >< dst\_inc >< N >$$

where the associated parameters are respectively: the addresses of the source and destination, the address step increments at the source and destination, and the number of 32-bit words to be transferred. Specific commands are also implemented for direct communication with the ComBlock. This architecture allows the implementation of macros using the UDMA commands. A list of all the UDMA commands and Macros implemented for this application is shown in Table 4.3.

Table 4.3: List of UDMA commands and application specific Macros

	UDMA Specifc Commands	
READ_REG	WRITE_REG	UDMA
READ_RAM	WRITE_RAM	CHANGE_CB
READ_MEM	WRITE_MEM	LOG
READ_FIFO	WRITE_FIFO	BUFF_SIZE
PicoAmmeter Macros	**HV Supply Macros**	**Histogram Generator Macros**
ADC500_CFG_FUNC	HV_SET	HISTO_CLEAN
DEC_CFG	HV_PWRDWN	HISTO_SET
PAMP_INIT	VMON_READ	HISTO_ENABLE
VADJ_SET	IMON_READ	HISTO_READ
PAS_SET		HISTO_RDCOUNT
PAMP_POT		HISTO_ISDONE
PAMP_TEMPS		
PAMP_GEN_HISTO		
PAMP_GET_HISTO		

These macros are used to control the firmware blocks described in Section 4.1.1. The names of the macros are self explanatory and provides an easy way to configure the HVPSS.

Application Specific Software: Temperature and Pressure Correction

The voltage corrections to preserve the detector gain, as a function of the environmental variables, are calculated and applied in the software running in the μP. The correction algorithm depends on the detector characteristics and it is the result of a dedicated laboratory tuning exercise provided in [50] where the following equation is introduced:

$$V(P,T) = V_0 \left(1 + \frac{1}{2}\left(\frac{P}{P_0} \cdot \frac{T_0}{T} - 1\right)\right) \tag{4.17}$$

where V is the voltage, P is the absolute pressure, T is the absolute temperature in degrees Kelvin and V_0, T_0 and P_0 are the reference conditions. $V(P,T)/V_0$ is the compensation factor.

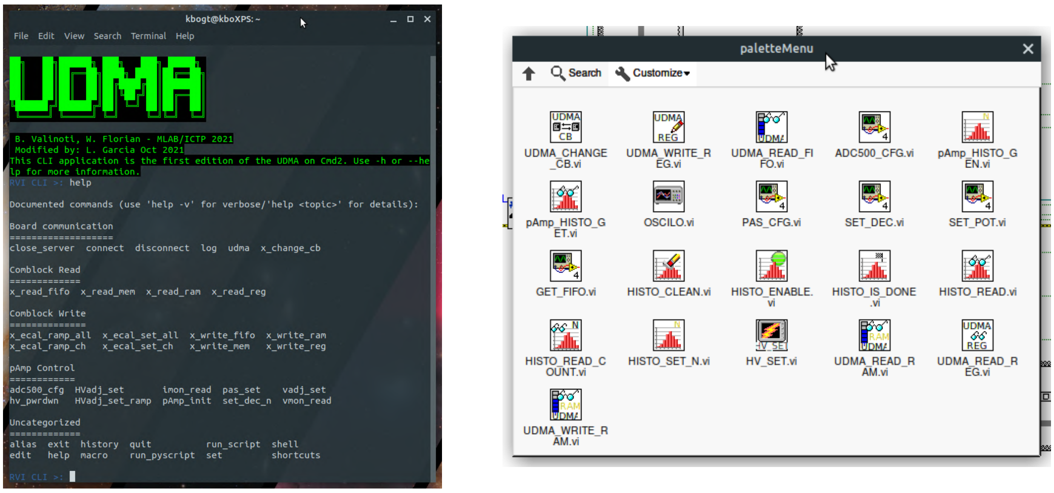
The Cortex-A9 μP provides a native IIC interface which is used to measure the data from the temperature and pressure sensors. The pressure sensor provides six calibration parameters needed to calculate the compensated pressure value [73]. This correction is done periodically as a task in the μP and can be enable or disable by the macro *HV_SET*.

4.3 The Control Software and Remote Communication

The HVPSS is controlled from a computer (PC) by TCP commands following the UDMA communication scheme. The command set is described in Table 4.3 and follows the UDMA syntax. The communication to the PC is done by transmitting the commands via TCP/IP. The latest version of the HVPSS can be controlled by a Python based Command Line Interpreter (CLI) [91] and through a library created for LabView [92]. Both interfaces are shown in Fig.4.13 with the different available commands displayed.

The HVPSS in its latest version is controlled from a PC by a graphical user interface (GUI). The GUI uses UDMA commands to communicate with the μP and to organize the control of different instruments. The GUI controls, in its current version, are divided in:

- ADC and Decimation Control: Control and monitor the HSADC status and sets up the decimation factor for the input to the oscilloscope.
- pAmp Ctrl: Provide control of the range and offset of the picoammeter board.
- Oscilloscope: Return an output of the oscilloscope signal as well as the controls and number of samples to manage in the GUI.



```
kbogt@kboXPS: ~
File  Edit  View  Search  Terminal  Help

UDMA

 B. Valinoti, W. Florian - MLAB/ICTP 2021
 Modified by: L. Garcia Oct 2021
This CLI application is the first edition of the UDMA on Cmd2. Use -h or --he
lp for more information.
RVI CLI >: help

Documented commands (use 'help -v' for verbose/'help <topic>' for details):

Board communication
===================
close_server  connect  disconnect  log  udma  x_change_cb

Comblock Read
=============
x_read_fifo  x_read_mem  x_read_ram  x_read_reg

Comblock Write
==============
x_ecal_ramp_all  x_ecal_set_all  x_write_fifo  x_write_ram
x_ecal_ramp_ch   x_ecal_set_ch   x_write_mem   x_write_reg

pAmp Control
============
adc500_cfg  HVadj_set       imon_read  pas_set    vadj_set
hv_pwrdwn   HVadj_set_ramp  pAmp_init  set_dec_n  vmon_read

Uncategorized
=============
alias  exit  history  quit          run_script  shell
edit   help  macro    run_pyscript  set         shortcuts

RVI CLI >:
```

(a) CLI Terminal

(b) LabView library palette

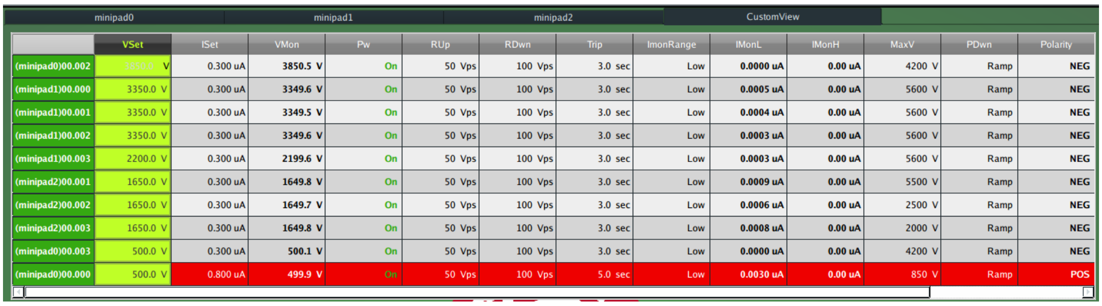
Figure 4.13: UDMA PC software interface.

- Histogram: Includes the input controls of the number of values to produce the histogram and a start-of-count button returning the histogram plot.
- Temperature and Pressure Log: Logs the temperature and pressure and enables the TP correction on the HV.
- Configuration: IP address, port, status, and calibration parameters.
- HV Setup and monitoring: This is a separate window that provides the HV control, V_{mon}, and I_{mon} plots.

The multichannel GUI is inspired in the CAEN General Control Software (GECO) adding a controller panel for each HV channel, a comparison between both is shown in Fig. 4.14.

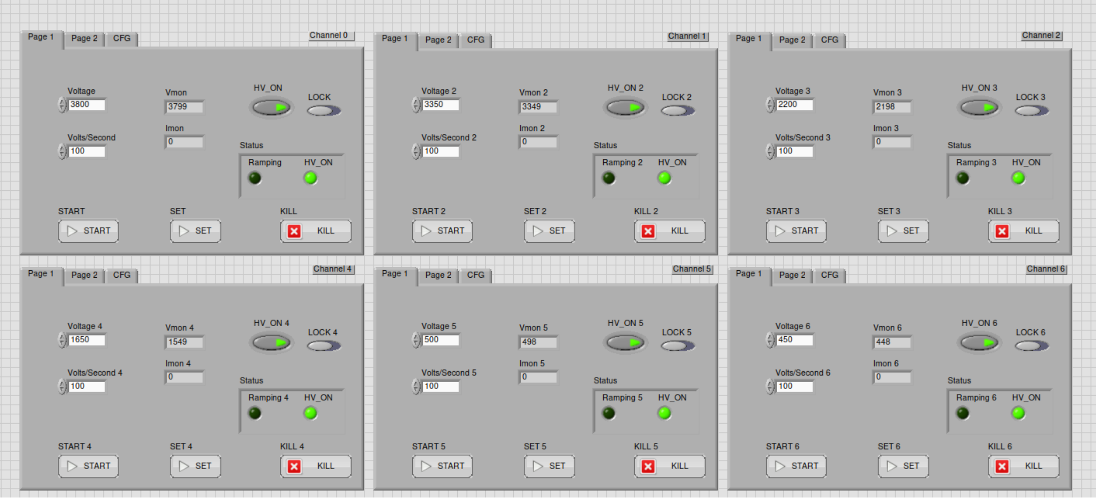
4.4 Summary

This chapter describes the firmware architecture that controls the hardware modules, processes the acquired data and handles the communication of a HVPSS channel with a PC and among other channels.



	VSet	ISet	VMon	Pw	RUp	RDwn	Trip	ImonRange	IMonL	IMonH	MaxV	PDwn	Polarity
(minipad0)00.002	3850.0 V	0.300 uA	3850.5 V	On	50 Vps	100 Vps	3.0 sec	Low	0.0000 uA	0.00 uA	4200 V	Ramp	NEG
(minipad1)00.000	3350.0 V	0.300 uA	3349.6 V	On	50 Vps	100 Vps	3.0 sec	Low	0.0005 uA	0.00 uA	5600 V	Ramp	NEG
(minipad1)00.001	3350.0 V	0.300 uA	3349.5 V	On	50 Vps	100 Vps	3.0 sec	Low	0.0004 uA	0.00 uA	5600 V	Ramp	NEG
(minipad1)00.002	3350.0 V	0.300 uA	3349.6 V	On	50 Vps	100 Vps	3.0 sec	Low	0.0003 uA	0.00 uA	5600 V	Ramp	NEG
(minipad1)00.003	2200.0 V	0.300 uA	2199.6 V	On	50 Vps	100 Vps	3.0 sec	Low	0.0003 uA	0.00 uA	5600 V	Ramp	NEG
(minipad2)00.001	1650.0 V	0.300 uA	1649.8 V	On	50 Vps	100 Vps	3.0 sec	Low	0.0009 uA	0.00 uA	5500 V	Ramp	NEG
(minipad2)00.002	1650.0 V	0.300 uA	1649.7 V	On	50 Vps	100 Vps	3.0 sec	Low	0.0006 uA	0.00 uA	2500 V	Ramp	NEG
(minipad2)00.003	1650.0 V	0.300 uA	1649.8 V	On	50 Vps	100 Vps	3.0 sec	Low	0.0008 uA	0.00 uA	2000 V	Ramp	NEG
(minipad0)00.003	500.0 V	0.300 uA	500.1 V	On	50 Vps	100 Vps	3.0 sec	Low	0.0000 uA	0.00 uA	4200 V	Ramp	NEG
(minipad0)00.000	500.0 V	0.800 uA	499.9 V	On	50 Vps	100 Vps	5.0 sec	Low	0.0030 uA	0.00 uA	850 V	Ramp	POS

(a) General Control Software (GECO) from CAEN HV power supply.



Channel 0
Voltage 3800
Vmon 3799
Volts/Second 100
Imon 0

Channel 1
Voltage 2 3350
Vmon 2 3349
Volts/Second 2 100
Imon 2 0

Channel 2
Voltage 3 2200
Vmon 3 2198
Volts/Second 3 100
Imon 3 0

Channel 4
Voltage 4 1650
Vmon 4 1549
Volts/Second 4 100
Imon 4 0

Channel 5
Voltage 5 500
Vmon 5 498
Volts/Second 5 100
Imon 5 0

Channel 6
Voltage 6 450
Vmon 6 448
Volts/Second 6 100
Imon 6 0

(b) HVPSS Control Interface, LabView

Figure 4.14: GUI comparison between CAEN and HVPSS.

The OSFA-UDMA architecture provides a pre-built full-stack slow-control for the user to develop different control blocks around it. All the FPGA blocks of the HVPSS were custom-designed as RTL blocks in VHDL and can be organized into one of these categories: Hardware-interface blocks (Section 4.1.1), PTP Synchronization and Local Time Manager (Section 4.1.2), Fast transient capture blocks (Section 4.1.3), data processing blocks (Section 4.1.4), and FPGA/μP communication blocks (Section 4.1.5).

A real-time operating system (FreeRTOS) runs in the μP to keep precise time control of multitasks. The μP runs hardware services by an Ethernet connection handled by a task. Another task provides a list of UDMA commands and macros to control the HVPSS. The μP also manages non-time-critical tasks such as temperature and pressure measurements using the native IIC interface as well as the calibration of the pressure sensor and the HV dynamic compensation.

Finally, the HVPSS is controlled by an external PC via Ethernet connection. The UDMA commands allows to configure each HVPSS channel using a python-based CLI or a LabView GUI. Custom made macros and a LabView function pallet were created for this application specifically.

In a similar way as in Chapter 3, many tests and iterations of the different blocks and software were done before the final implementation on the HVPSS. All the tests were performed under lab conditions at ICTP and INFN and under Test Beam conditions at CERN. The results of these tests are detailed in Chapter 6.

Chapter 5

Data Acquisition System Design for Water Cherenkov Detectors

Many of the components described in Chapters 3 and 4 have several applications in a different context than the multi-channel HVPSS. Concerning high-energy particle detectors, most of them have similar needs to those presented for MPGDs. In the context of indirect detection of cosmic rays and gamma ray bursts (GRBs), high-resolution timing to accurately correlate the data corresponding to specific events is necessary, as their duration may be in the scale of hundreds of nanoseconds and the time between events are in the same order of magnitude.

Extensive particle showers are detected combining the measurements of several detector units over a wide area. Accurate timing in cosmic ray detection is critical for reconstruction of events from multiple scattered detectors. Since most of the detectors dedicated to study cosmic rays generate continuous analog signals, a precise timing depends on the sampling rate and the subsequent triggering system operating on the generated digital data stream.

SoC-FPGA devices represent the state-of-art technology nowadays, which combines the versatility of high-level programming of a microprocessor with the parallelism and high-speed of a reconfigurable FPGA device in a single chip. This fusion of technologies enables the detectors to fully digest raw real-time data into processed information, allowing scientists to design higher precision instruments in smaller devices grabbing more data and reducing dead-time, thus increasing the measurement reliability of the experiments.

The modular design combined with the reconfigurable properties of the SoC-FPGA and the portable architecture described in Section 4.3 allows the adaptation of the HVPSS channel into a Data Acquisition System (DAQ) front-end for Water Cherenkov Detectors (WCD). Indeed, most of the system components have been used as the front-end DAQ for WCD (DAQ-WCD) to conduct experiments for studies and detection of astrophysical high-energy sources in collaboration with the School of Physics and Mathematics Sciences of San Carlos University in Guatemala (ECFM-USAC).

The main DAQ requirements for cosmic rays studies using WCD are the following:

- Nanosecond data acquisition for pulse-shape analysis.
- Online pre-processing of incoming data and data conditioning for storage.
- Temperature and pressure readout for baseline correction.
- HV power supply control with real-time temperature and pressure compensation.
- A Global Positioning System (GPS) module control and readout of position and timing as well as time synchronization based in the pulse-per-second (PPS) signal.
- Ethernet communication for remote data handling and control.

Even if most of these requirements are already solved with the HVPSS, some specific modifications were needed for the front-end DAQ-WCD. This chapter starts describing the main components of a WCD station and the experimental setup used in ECFM-USAC (Section 5.1), the modifications done in the HVPSS needed to build the DAQ-WCD (Section 5.2), and the CR studies based on pulse shape discrimination (PSD) carried in the framework of this thesis (Section 5.3).

5.1 Water Cherenkov Detector Station Components

Water Cherenkov Detectors is a type of particle detector designed to capture the Cherenkov photons produced by the interaction of a high-energy charged particle ($\geq$ 500 MeV) traveling at speeds closer to speed of light.

The general structure of a WCD ground station similar to the ones used in experiments like Auger [18], LAGO [17] and HAWC [19] consists of a water tank with a reflective inner surface, several photomultiplier tubes (PMT), communication electronics, power supply electronics, and DAQ electronics. One example of a WCD surface detector station used in the Piere Auger observatory is shown in Fig. 5.1.

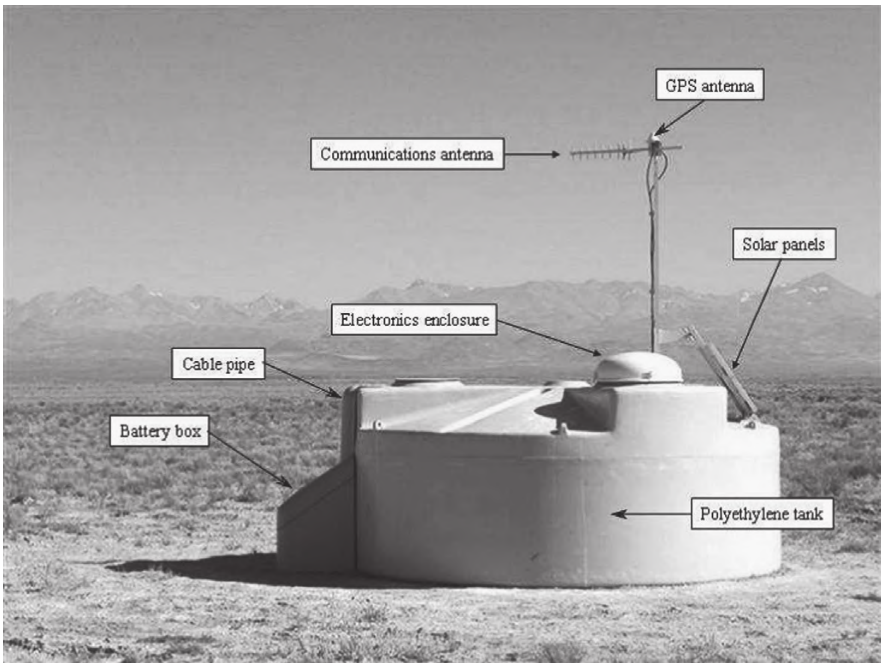


Figure 5.1: Surface detector station used in Piere Auger Observatory [18].

Cherenkov production is relatively efficient in water due to its high index of refraction. The interaction of a high-energy particle crossing the volume of water produces Cherenkov photons. A reflective inner tank wall material helps to collect the photons by the PMTs. A front-end digitizes the analog signal and condition it for feature extraction.

A ground-based WCD experimental tank was set up in the Instrumentation Laboratory of the ECFM-USAC. The test platform is composed of a 220 liters tank covered with Tyvek as a reflective material on the inside walls and light-proofed with the bituminous membrane on the outside. Light is collected using a Photonis XP1802 [93] PMT. The front-end electronics provide the HV needed to polarize the PMT, temperature, and pressure measurements for baseline compensation on the PMT [94].

The experimental setup is shown in Fig. 5.2. The setup is build with the following parts:

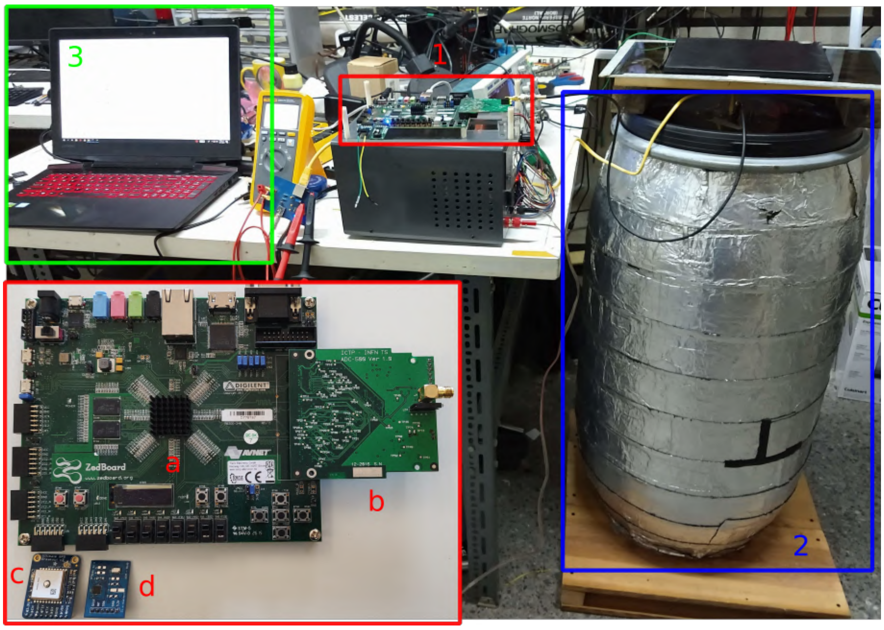


Figure 5.2: Experimental Setup ECFM-USAC.

1. Data acquisition system
    (a) Zedboard commercial board.
    (b) ADC500 Board.
    (c) GPS Module.
    (d) Pressure and Temperature sensors.
2. Water Cherenkov Detector station.
3. PC for data storage.

5.1.1 Photomultipler Tube

A PMT is a light-sensitive detector multiplying the current produced by incident light as much as 10^7 (140 dB). These detectors multiply the current produced by the incident light in multiple dynode stages. The sensitivity of these detectors is ideal for single-photon counting.

In Fig. 5.3 is shown the schematic view of a PMT working principle (Hamamatsu 2021 [95]). The incident light ejects an electron in the photo-cathode consequence of the photoelectric effect.

These electrons are directed to a dynode (electron multiplier) by a focusing electrode producing secondary electrons. A HV electrical field is applied in each dynode stage to guide and multiply the number of electrons in each stage. The electron cascade is collected by the anode producing a current which can be read by the electronics.

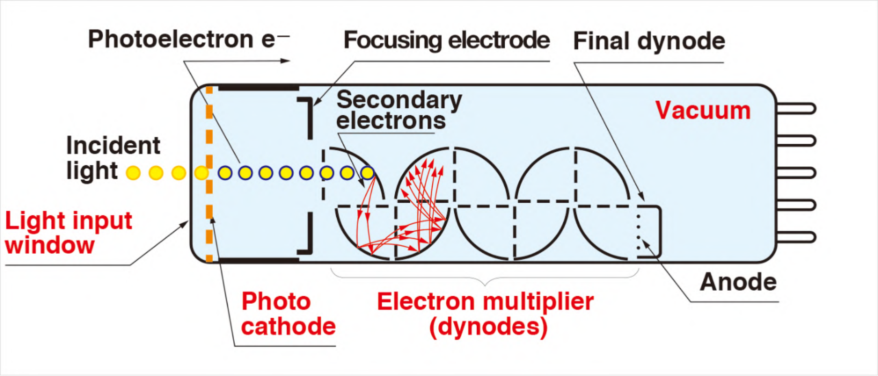


Figure 5.3: Schematic view of a photomultiplier tube working principle [95].

5.2 DAQ Platform Based on SoC-FPGA

As mentioned at the beginning of this chapter; several components described in Chapters 3 and 4 are used in this application. This section describes the hardware and the firmware implementation needed for the DAQ-WCD system as well as the custom modifications done to achieve the established requirements.

5.2.1 External Hardware Requirements

A single pulse produced by cosmic rays in a WCD has a typical duration of 100-200 ns. To digitize these pulses, the system consists of a high-speed analog to digital converter, able to manage 8-bit data resolution, 500 MHz sampling rate (Section 3.1.3).

To polarize the dynodes of the PMT (Section 5.1.1), a HV power supply with range from 0 to -2000 V is needed. The DC/DC supply board (Section 3.1.1) is used for this purpose. The HV range is lower than the voltage range for the HVPSS, therefore the HV in the DAQ-WCD is limited by software. However, the DC/DC supply board is fully-compatible with the

BPn2020512 which is a 2 kV power supply to substitute the BPn4010512 4 kV used.

Temperature and pressure (PT) sensors are needed for baseline correction. The knowledge of the baseline level is crucial in experiments like LAGO, where is intended to measure the rate or particles at ground level with great accuracy. Baseline in the PMT shifts depending on ambient pressure and temperature as described in [94]. The temperature and pressure hardware and control is kept changing the connector to a PMOD [60] compatible board as shown in Fig. 5.2.

A commercial GPS, MTK3339 chipset built in an Adafruit breakout board provides the time synchronization among different stations [96]. The PPS output from the GPS board is synchronized with the satellite time and provides a time reference known in the system as slow-clock.

The main difference from the HVPSS is the SoC-FPGA selection. The DAQ-WCD firmware is developed in a Zynq-7020 carried in a Zedboard commercial board [77]. The Zedboard connects with the high-speed ADC500 by its FMC-LPC connector. The PT sensors and the GPS interface through one of its four PMOD connectors. The firmware design is described in Section 5.2.2

5.2.2 Firmware Development

Fig. 5.4 shows the firmware design corresponding to the DAQ-WCD system. The design keeps the UDMA architecture described in Section 4.3. However, it is significant smaller than the one presented for the HVPSS (Fig. 4.2).

FPGA Firmware

Two hardware interface drivers from the HVPSS are kept in the DAQ-WCD system design: the *ADC Driver* and the *HV SPI interface* (more details in Section 4.1.1). The data processing blocks are also kept to provide visualization tools and eventually to create a power spectrum using the Histogram Generator Block.

The first difference from the previous design is the PPS Synchronization block. The 250 MHz synchronization clock coming from the ADC is synchronized with a PPS signal provided by the GPS. Both are used to generate a global clock inside a *Timestamp Generator* block. This block returns two 32-bit counters, a slow counter that keeps track of the PPS count in

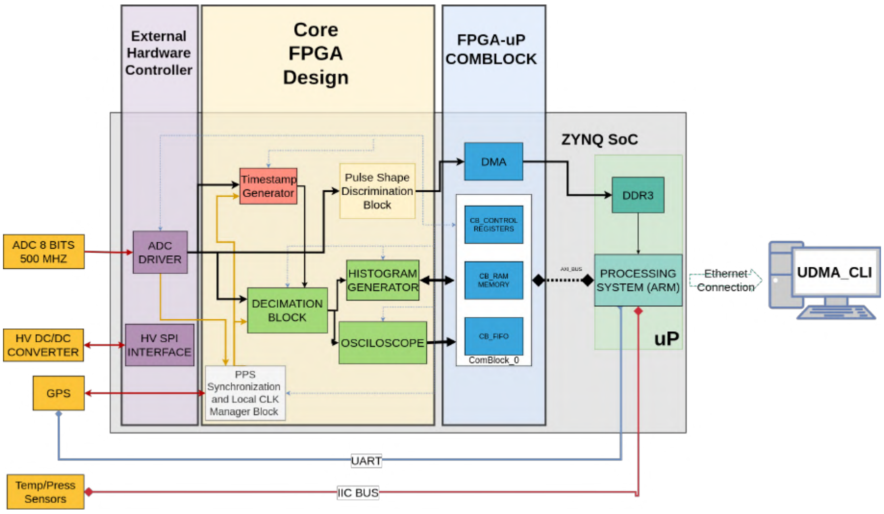


Figure 5.4: Block Diagram of FPGA firmware design for DAQ-WCD.

seconds, and a fast counter which counts the number of cycles of the synchronization clock from the ADC. The fast counter is cleared in each PPS rising edge as shown in Fig. 5.5.

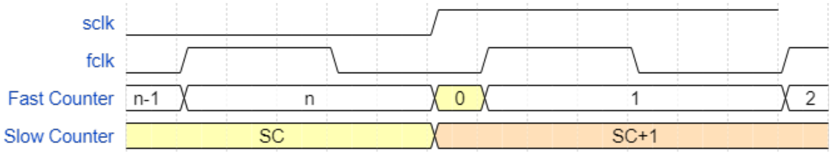


Figure 5.5: Local time synchronization done by the PPS block.

The second addition is the pulse shape discrimination block created to characterize the different type of pulses corresponding to different type of particles. This block is described with more detail in Section 5.3.

μP Firmware

The μP runs FreeRTOS keeping with the UDMA architecture (see Section 4.2). The temperature and pressure sensors control task is kept.

The GPS module driver was added to the application specific tasks of the μP. The communication with the GPS is by an UART interface using the multiplexed input/outputs (MIO) from the μP. The μP enables the PPS from the GPS module at power up, and read the time and location on the station. The communication with the board is via Ethernet with the same commands described in Section 4.2.

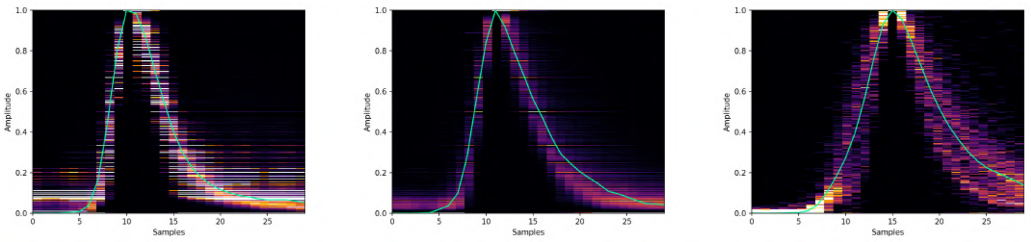
5.3 Pulse Shape Discrimination

WCDs have different signal response depending of the type of particle. Some of the different types of signals are listed below [22].

- Electrons usually drop all their energy in the detector, giving a signal proportional to their energy.
- Photons usually convert into an electron-positron pair within the water volume, and then the secondaries radiate all their energy. In the end, the signal is again proportional to the energy of the incoming particle.
- Muons on the other hand go through the detector without loosing all their energy (expect in the rare muon decay cases). The signal is then proportional to the track length in the detector, and no longer to the particle energy.

Further detail of the pulse response related to the interaction of the particles with the mater is explained in Chapter 1. The variation in the amount of light produced by each particle can be used to distinguish them [97]. Pulse shape discrimination (PSD) is a typical classification problem whereby digitised waveforms can be discriminated based on their time and energy features [98]. With enough number of samples it is possible to do PSD by doing correlation of an incoming signal with a normalize representative pulse of each type of particle. An objective way of classifying the pulses is by grouping them by their similarities. This classification can be done with a k-means or a centroid-based-cluster algorithm [99]. An ideal representative pulse is the one which has in average the same correlation distance with the rest of the pulses. Or at least, that the correlation distance is far enough to be discriminated. By applying standard normalization, it is possible to obtain a representative pulse with average correlation distance to the rest of the cluster [100].

Fig. 5.6 shows a heat map of three different types of pulses from the RAW data captured with the experimental setup. The representative pulse is the average pulse of each cluster, scaled to 1 and aligned to the maximum value. Overlaid in each map (also scaled to 1) is the typical pulse obtained by averaging the standard score of all the pulses in the cluster.



(a) Type 0 (b) Type 1 (c) Type 2

Figure 5.6: Heat map of pulses (scaled to 1) found in the cluster and typical pulse obtained by standard score for each cluster.

The pulses correlation matrix is shown in the table 5.1. To compensate for the high correlation between types 0 and 1, a voting system will also extract the amplitude of the pulse for the final decision.

Table 5.1: Pearson Correlation between the three selected pulses

	Type 0	**Type 1**	**Type 2**
Type 0	1.0000	0.9600	0.7744
Type 1	0.9600	1.0000	0.8360
Type 2	0.7743	0.8360	1.0000

PSD is done by correlating an input pulse from a detector and the representative pulses for the different types of particles. The results of the Pearson correlation are compared to identify the type of particle with the maximum correlation. The discrete convolution to obtain the correlation is implemented in hardware by using a Finite-Impulse Response (FIR) filter.

The Pearson correlation function between a pair of N-element data vectors is stated in Eq. 5.1, where x is the input signal and y the reference pulse, $\bar{x}$ and $\bar{y}$ are their respective average values, and σ_x and σ_y are their corresponding standard deviations. The result $\rho(x, y)$ is closer to 1 when the likelihood between both signals is closer.

$$\rho(x,y) = \frac{\sum_{i=0}^{N-1}[(x_i - \bar{x})(y_i - \bar{y})]}{\sigma_x \sigma_y} = \frac{1}{\sigma_x} \sum_{i=0}^{N-1} \left[(x_i - \bar{x}) \left(\frac{y_i - \bar{y}}{\sigma_y} \right) \right] \tag{5.1}$$

If the reference signal is static, y_i, $\bar{y}$ and σ_y are constants. This expression $((y_i - \bar{y})/\sigma_y)$ is the standard score normalization, and it will be used to calculate the coefficients of the FIR (c_i). To avoid using floating-point coefficients, the result is multiplied by a scaling factor of n bits, as shown in Eq. (5.2). To establish a good reference signal, a large number of previously classified pulses are normalized using the standard score and averaged for each point. For this experiment, each reference (electron and muon) was created using 42,000 pulses, and the coefficients have a scaling factor of $n = 14$.

$$c_i = \frac{y_i - \bar{y}}{\sigma_y} 2^n \tag{5.2}$$

Pulse selection based on Pearson correlation analysis was implemented taking advantage of a Tapped delay FIR line from a Xilinx FIR v7.2 core [101], configured on Systolic Multiply-Accumulate architecture. Three FIR filters, one for each cluster, are set in parallel in free-running mode connected to a voting system where the pulse will be identified and tagged. The FIR coefficients are calculated based on a representative pulse of each cluster.

The signal will be processed in parallel by two FIR filters with its corresponding reference. Because σ_x and $\bar{x}$ will be the same for both FIR inputs, the correlation for both filters are scaled in the same proportion. The selection logic then can be simplified to take the output of both filters and make a decision based on the higher correlation through the duration of a pulse, establishing a rejection threshold. Taking this into consideration, the output of the filter is defined by Eq. (5.3).

$$\rho_{out} = \sum_{i=0}^{N-1} x_i c_i \tag{5.3}$$

5.3.1 Preliminary Tests: Muon-Electron PSD for WCD.

The first test was done using a data set collected from the experimental station before using the DAQ-WCD system. The signal was sampled at 125 MHz with 14-bit resolution using a Red Pitaya on-board ADC [102]. This test aimed to discriminate between two different types of particles: muons and electrons. This section describes the FIR-based correlation design process up to the implementation in the SoC-FPGA.

Feature extraction was performed in the incoming signal to obtain the rise time (10% to 90% of the output step height) and the amplitude needed to discriminate among the different types of signals. In Fig. 5.7, a typical distribution of the pulses captured with WCD is presented. To have an objective classification criteria, we run a k-means clustering algorithm of four partitions (Figure 5.8) to select the border parameters to differentiate the signals.

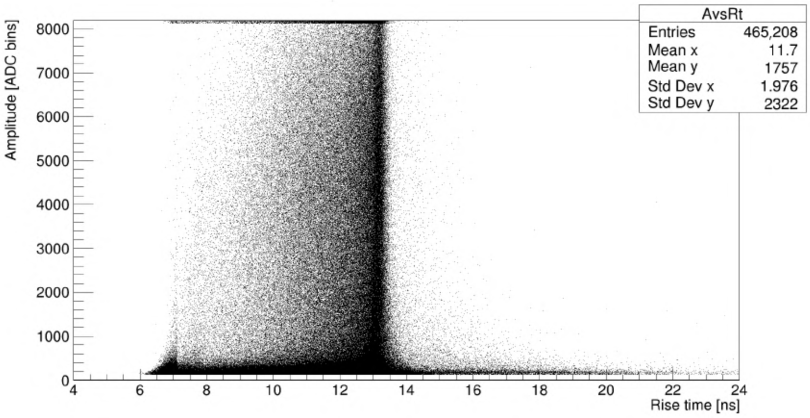


Figure 5.7: Amplitude vs. rise time of typical pulses captured with WCD.

The classification criteria selected for the pulse shape discrimination is the following:

- Electron: amplitude below 3000 - Rise time: between 6 and 9 ns.
- Muon: amplitude from 3000 to 8000 - Rise time: between 11 and 15 ns.
- Electrical Discharge: amplitude greater than 8000 or data that do not fall in the previous categories.

To validate our criteria, we study the physics of the muon decay phenomenon [103]. The muon mean lifetime is 2.196 μs, and it was used to determine the reference pulses corresponding to a typical muon and electron. Because charge must be conserved, one of the products of muon decay is always an electron. This can be used in such a way that pairs of pulses whose time difference fits the model were searched to use as reference, as we can observe in Fig. 5.9. This procedure has been used in another context to measure muon half-life [104].

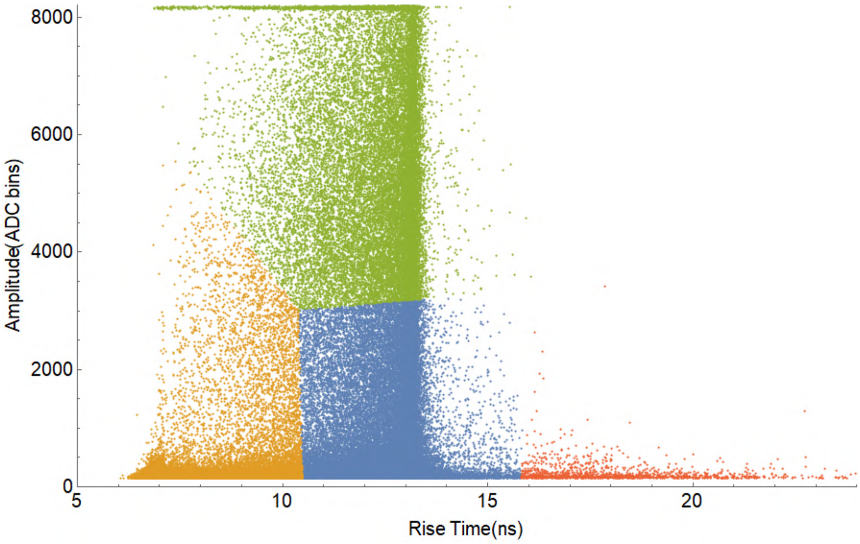


Figure 5.8: K-means (4) cluster analysis for boundaries selection. Orange: electrons, green: high amplitude muons and electrical discharges, blue: low amplitude muons, red: other type of signals.

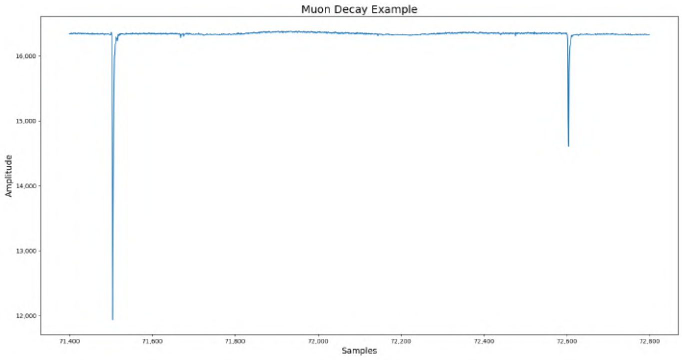


Figure 5.9: Example of muon–electron decay.

Moreover, the muon has higher mass than the electron (˜200 times more). Having a much greater mass, the muon can travel further into the medium producing longer pulses. Because electrons have lower mass, they interact more in the medium, which makes them deposit their energy more quickly, producing shorter pulses. A similar discussion was also presented by

Salazar [105].

The ground truth for each pulse is indicated by assigning an identification value for each type of signal: 0 for electron, 1 for muon, and 2 for electric discharge, as shown in Fig. 5.10.

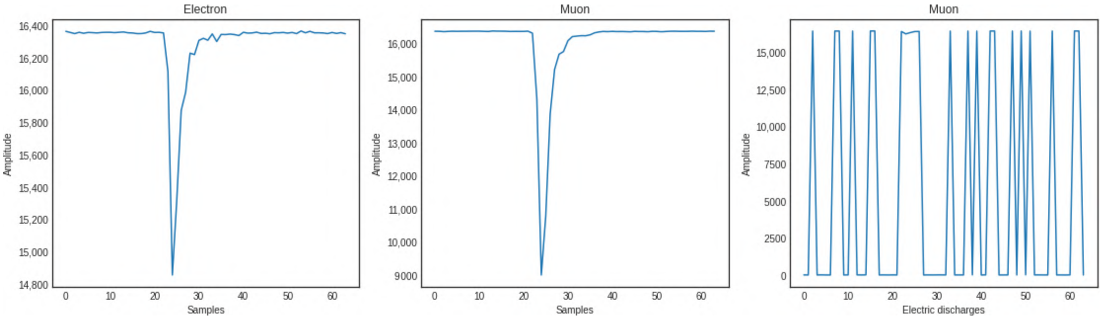


Figure 5.10: Different types of signals: electron, muon and electric discharges.

As seen in Fig. 5.7, the main criteria to differentiate between muons and electrons are the rise time and the amplitude of the pulses. The first criterion to classify the signals is the rise time of the pulse. This is difficult to achieve due to the DAQ sampling time of 8 ns, which is smaller than the rise time of the electron. To overcome this problem, we study the overall form of the pulse to perform the selection. A comparison between electron and muon reference pulse normalized in amplitude to 1 to highlight their differences is shown in Fig. 5.11. At the current sampling rate, the peak of the electron is reached by only one data point. In contrast, a muon may have two or three data points before reaching the peak; these variations give the muon reference a “flattened” peak shape. A slower rise time has the effect of a smoother curve after the peak. The correlation between both references is 0.62; if we set a correlation value of 0.9 or higher to accept a pulse as a particle, the differences between the pulses is enough to use them as a criteria of classification.

The amplitude of the pulses is the second criteria used to make a decision. As is shown in Fig. 5.8, electrons typically have lower amplitude compared with muons (orange cluster). However, some muons may have low amplitude as well (blue cluster). At higher amplitudes (green cluster), it is possible to find muons and electrical discharges produced by the PMT. Some electrical discharges may saturate the signal, as it is seen in top of the green section of the cluster, making it easy to separate them from a muon. For the purpose of analysis, we will call the value that separates the amplitude between muon and electrons the muon threshold

(μ_T).

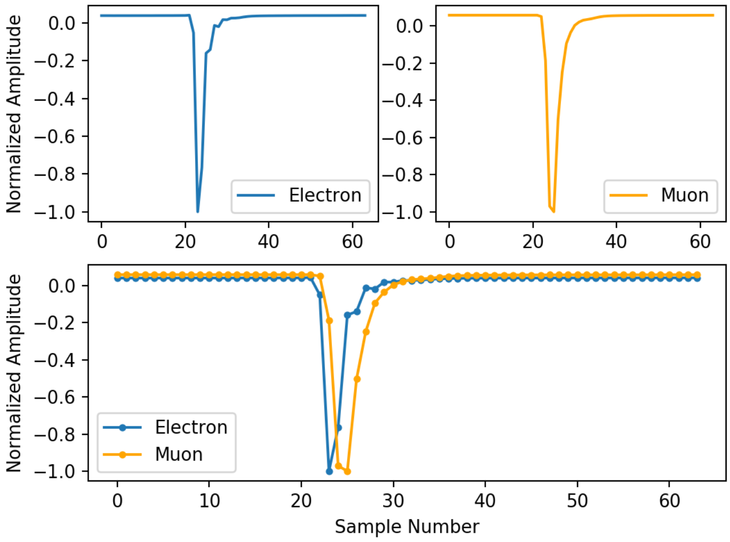


Figure 5.11: Typical electron and muon signal sampled at 125 MHz normalized in amplitude.

The selection logic decides that a pulse is starting by the crossing of a threshold by the signal. This will start a state machine that will search for the maximum amplitude of both the correlation results (ρ_μ and ρ_e) and the amplitude of the peak (P_x). When the signal crosses back the threshold, the state machine will consider it as the end of a pulse and perform a selection according to the collected information and the criteria established in the previous paragraphs. The selection criteria uses the following logic:

1. If ρ_μ and ρ_e are greater than a base reference value ($R \approx 0$) go to the next criteria. This discards uncorrelated signals like electrical discharges.

2. If $\rho_e > \rho_\mu$, the signal is an electron, else if $\rho_\mu > \rho_e$, the signal is a muon.

3. In the case of $\rho_e = \rho_\mu$, the amplitude of the peak P_x is used to take the decision. If $P_x \geq \mu_T$, the result is a muon.

4. If the signal is in saturation ($P_x = \max(x)$), the selection logic classifies it as an electrical discharge.

SoC-FPGA Implementation

A block diagram of the muon–electron correlation discriminator is shown in Fig. 5.12. The FIR filter is used to do the correlation of the input signal with an output result given by Eq. (5.1). The coefficients are calculated by standard score normalization and averaging typical signals like the ones in Fig. 5.10 using Eq. (5.2).

The design was implemented and tested on Xilinx FPGA System on Chip (SoC) devices: ZU9EG Zynq UltraScale+ (ZCU102 Development Board [106]) and ZC7Z020 Zynq (Zedboard). The implementation in the Ultrascale SoC is for further comparison with an Artificial Neural Network (ANN) as part of studies in Muon-Electron PSD based on SoC for WCD [107].

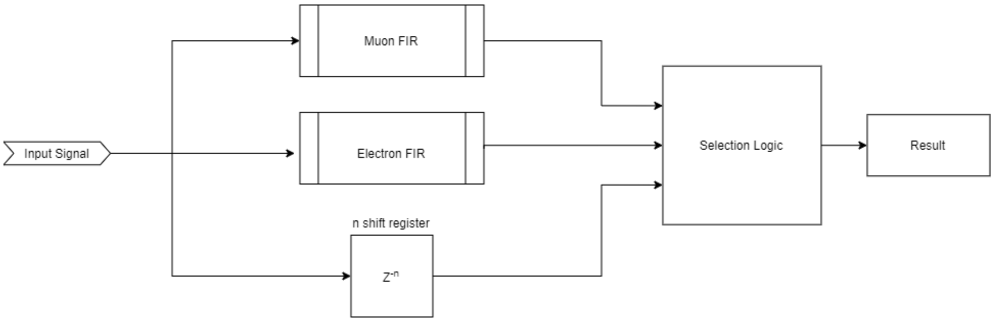


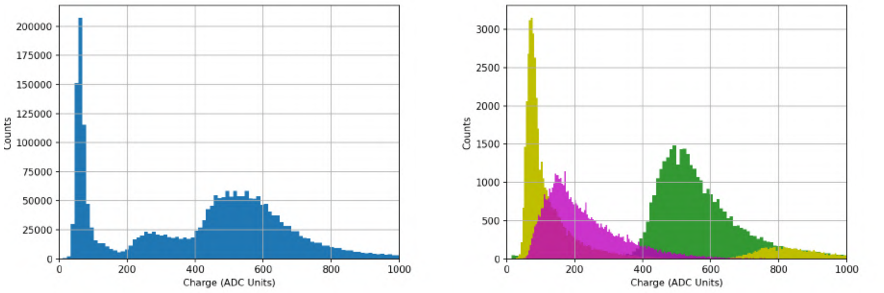
Figure 5.12: Block diagram of FIR-based correlation pulse discriminator.

A RAM-based shift register block provides the latency to the signal to align it with the outputs of the filters to be used as inputs in a selection logic block. The selection logic state machine starts when the input signal crosses a threshold. It is implemented as a peak holder until the signal crosses down the threshold again. The selection logic is done in parallel until this moment. After the signal crosses down the threshold, the result will be available in the next clock cycle, indicated by a *ready* signal. After this, the system is ready to receive another pulse. The possible outcomes are 0 for electron, 1 for muon, 2 for electrical discharge, and 3 for other type of signal.

After the preliminary test, further studies were conducted using data sampled with the DAQ-WCD system. The first approach was to find different types of pulses in the collected data. Although several clusters may be found, the criteria to determine if corresponds to a particle depends of the figure of merit as explained in the next section.

5.3.2 Figure of Merit

To establish the capabilities of our system in isolating different particles, a standard figure of merit (FOM) was used [97]. The FOM was established by computing a charge histogram of the acquired data and selecting the bins with higher charge counts. In Fig. 5.13a it is possible to distinguish two different types of pulses, the first located between the 200 and 400 units of charge, and the second between 500 and 700 units. With this information we selected the clusters that contribute the most counts to the charge in the two established regions as shown in Fig. 5.13b. These clusters will become the ground truth for calculating the FIR coefficients.



(a) Charge integration histogram (b) Charge contribution of each cluster

Figure 5.13: Charge contributions expressed in integrated ADC channel units

Further analyses are needed to do a precise determination of the particles that corresponds to each cluster. However, based on the work of Salazar [108] as reference we estimate that the area tagged in yellow may be mostly formed by electrons. The area tagged in magenta may correspond to inclined muons, and the green area may correspond with vertical muons. A precise determination requires more studies that are out of the scope of this thesis.

Other differences among the pulses are shown in Fig. 5.14 where it can be distinguished the relation between the rise time and amplitude of the selected clusters. The first thing to notice is the divergence of rise time among the green cluster (type 2) and both yellow and magenta groups (type 0 and 1, respectively); the last two separate each other by a change in the amplitude. By further contrasting the slew rate and the amplitude is noticeable the dissimilarity in slopes among the three types of pulses, where the green cluster clearly shows different inclination than the other two clusters.

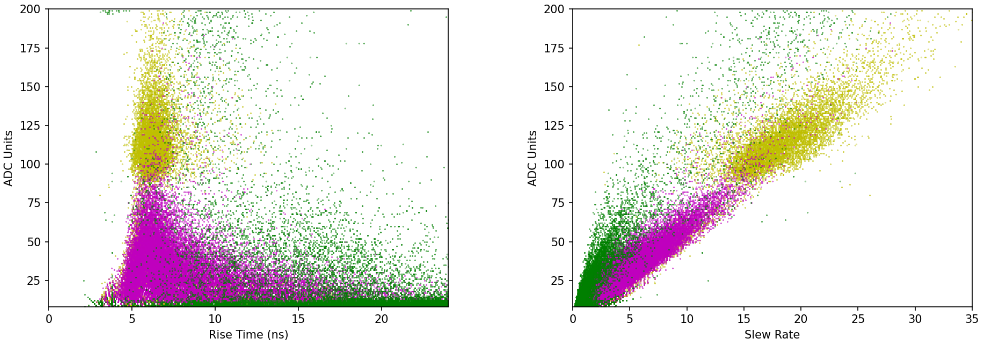


Figure 5.14: Rise Time vs Amplitude and Slew Rate vs Amplitude plots for the three selected clusters.

5.4 Summary

The front-end electronics used for indirect detection of cosmic rays and GRBs using WCD share many requirements with the HVPSS described in previous chapters. The modular design of the hardware elements and the reconfigurable capabilities of the SoC-FPGA allows the system to be used seamlessly as a DAQ for WCDs.

Several of the hardware blocks needed to reach the nanosecond synchronization, TP baseline correction, and HV power supply control were fully described in Chapters 3 and 4. This chapter describe the requirements in the electronics of a WCD station and the modifications needed to transition the HVPSS into a DAQ system for cosmic ray studies (DAQ-WCD).

The DAQ-WCD was tested in an experimental station in the School of Physics and Mathematics (ECFM-USAC) in Guatemala. A new block was implemented for Pulse-shape discrimination (PSD) in cosmic rays particles. This chapter describes the working principle of a FIR-based PSD method, the correlation distance calculation used to obtain the representative pulses corresponding to the different types of particles under study, and the implementation of the RTL block on the FPGA. A preliminary test for muon-electron PSD was done in two different SoC-FPGAs as a proof of concept for this method. A study of the figure of merit was done over a new data set collected with the DAQ-WCD to identify the types of particles that we are able to discriminate. The results of these tests are described in Chapter 6.

Chapter 6

Experimental Results

This chapter describes the most significant experimental results obtained after several tests of the hardware and software components of the HVPSS for MPGDs. As described in the previous chapters, many of the challenges solved by the designed hardware are applicable in the context of high-energy particle detectors specifically, for indirect measurements of cosmic rays where the flexibility of the design allows the HVPSS channel to be used as a DAQ for WCD. This chapter also describe the results obtained in this application.

As described in Chapter 2, the HV control and monitoring of a hybrid detector is a challenging task. The MPGD used in COMPASS-RICH-1 is divided into detector cells called sectors, each of which had six stages, three of gain and three of transmission. The gain in each stage depends of the HV applied between its electrodes. Each of the bias voltages are relative to the previous stage instead of ground. This correlation between voltages implies that every change in one of the stages needs to translate to the rest of the system. During normal operation electrical discharges may happen, depending on the discharge rate the bias voltage of an electrode can be reduced to guarantee safe operating conditions. The HVPSS aims to study the behavior of these fast transients and implement an active HV compensation to prevent them.

The HVPSS needs to be modular and scalable, with each channel providing a HV power supply to the electrode with low-noise and high-accuracy control. Current and voltage must be monitored and logged in real-time detecting high-speed transient events timestamping them and storing the information collected from them for further studies. To track the propagation of fast transient events between sectors and stages, high-speed electronics must be placed on each electrode. This implies that each HVPSS channel is placed in a different HV power domain, complicating the communication among them. This is important, as every channel must be synchronized with a common clock. A HV isolated network interface allows for a dedicated communication line for transmission of time synchronization information as well as time-critical commands among channels. Finally, the HVPSS must perform automatic corrective measurement for environmental variables such as pressure and temperature as well as others that may be important to prevent misbehaviour of the detector.

The complexity of a system that meets the specific conditions described leads to adopt a divide-and-conquer methodology during the design tree. This process started with a single channel instrument able to meet the high-speed timing constraints. The selection of a SoC-FPGA gave the flexibility and resources to be used as a base hardware platform for the design. A 500 MHz ADC was selected to digitize at high-speed the current measured from the electrode. To simplify the design process the bases of a portable framework architecture were proposed in 2019 leading to the publication of *Design for Portability of Reconfigurable Virtual Instrumentation* [90], becoming the bases that lead to the architecture described in Section 4.3.

A prototype was built and tested under lab conditions at the ICTP-MLAB and INFN Trieste laboratories before testing the complete system under beam conditions at CERN. Built over the OSFA framework described in Chapter 4, the developed prototype provides: a HV power supply for one electrode, current monitoring with pA resolution using a picoammeter board, fast-transient detection and timestamp with a local clock, pressure and temperature compensation in the HV, and signal analysis tools on the FPGA. The results of these tests and the exercise under the beam line at CERN were published in 2020 in the paper named *A scalable High Voltage Power Supply System with system on chip control for MicroPattern Gaseous Detectors* [57]. Thereafter, the paper *MPGD-based photon detectors for the upgrade of COMPASS RICH-1 and beyond* was published [45].

After the results of the test beam, the HVPSS channel was upgraded to the current revision described in Chapter 3. The new revision includes the design of a High Voltage Isolation Bidirectional Network Interface (HVIBNI) for communication among different channels. The results of the performance of the HVIBNI were presented in 2020 in the Applications in Electronics Pervading Industry, Environment and Society (APPLEPIES 2021) leading to the publication *High Voltage Isolated Bidirectional Network Interface for SoC-FPGA Based Devices: A Case Study:*

Application to Micro-pattern Gaseous Detectors [109]. The HVIBNI was used to communicate among channels through a privileged network used for time synchronization. A modified version of the Precise Time Protocol (PTP) standard was implemented using the HVIBNI achieving 20 ns time synchronization. The results were published in MDPI-Instruments on January 2022 in a publication called *Multichannel Time Synchronization Based on PTP through a High Voltage Isolation Buffer Network Interface for Thick-GEM Detectors* [110].

During the research process in the prototype building, several common links with cosmic rays detectors were found. Accurate timing in cosmic ray detection is critical for the reconstruction of events from multiple scattered detectors. Since most of the detectors dedicated to studying cosmic rays generate continuous analog signals, precise timing depends on the sampling rate and the subsequent triggering system operating on the generated digital data stream. A replica of the HVPSS channel prototype was tested in an experimental WCD station as part of the project "Studies and Detection of High Energy Astrophysics Sources" in Guatemala. This study was part of a collaboration with the School of Physics and Mathematics at San Carlos University (ECFM-USAC) in Guatemala. The first results lead to the publication *DAQ platform based on SoC-FPGA for high resolution time stamping in cosmic ray detection* [111] in the International Cosmic Ray Conference (ICRC 2019).

The data collected was used during these tests for studies on pulse-shape discrimination (PSD) using the front-end electronics of WCDs. These studies result to the publications *Muon electron pulse shape discrimination for water Cherenkov detectors based on SoC-FPGA* [107] (MDPI-electronics 2021) and *Pulse Shape Discrimination for Online Data Acquisition in Water Cherenkov Detectors Based on SoC-FPGA* [99] (PoS(ICRC2021) 2021), where the main contribution was the development of an RTL block for PSD based on a correlation technique using FIR.

This chapter is divided in three main sections: the tests and results of the common elements of the HVPSS and the DAQ-WCD from now and on in this chapter named as base system (Section 6.1), the specific tests related to the HVPSS for MPGDs (Section 6.2), and the specific tests related to the DAQ for WCDs (Section 6.3).

6.1 HVPSS and DAQ-WCD Base System Tests and Results

This section describes the most relevant tests related to the common elements for the HVPSS and the DAQ-WCD. The first prototype of the HVPSS is shown in Fig. 6.1 where the main components are described (see Chapter 3). This revision of the HVPSS became the base for the development of the DAQ-WCD. Some tests leading to the selection of the components were already discussed in Chapters 3 and 4.

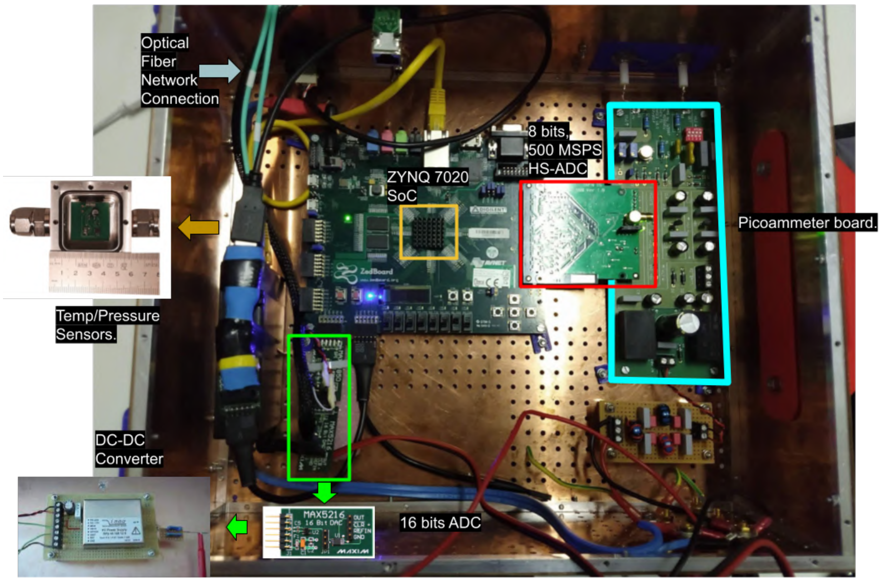


Figure 6.1: First prototype used during test beam at CERN

6.1.1 Pressure and Temperature Correction on the HV Power Supply

In both applications the HV power supply needs to have temperature and pressure compensation. In case of the HVPSS the HV is adjusted in real time according the Eq. 4.17, and in WCDs this compensation is specific for the PMT. In both cases, this compensation is done by a programmable task in the μP (see Section 4.3). The μP measures the pressure and temperature (PT), calculates the adjusted voltage and send the values to the FPGA to set the configuration voltage of the HV power supply board as shown in Fig. 6.2.

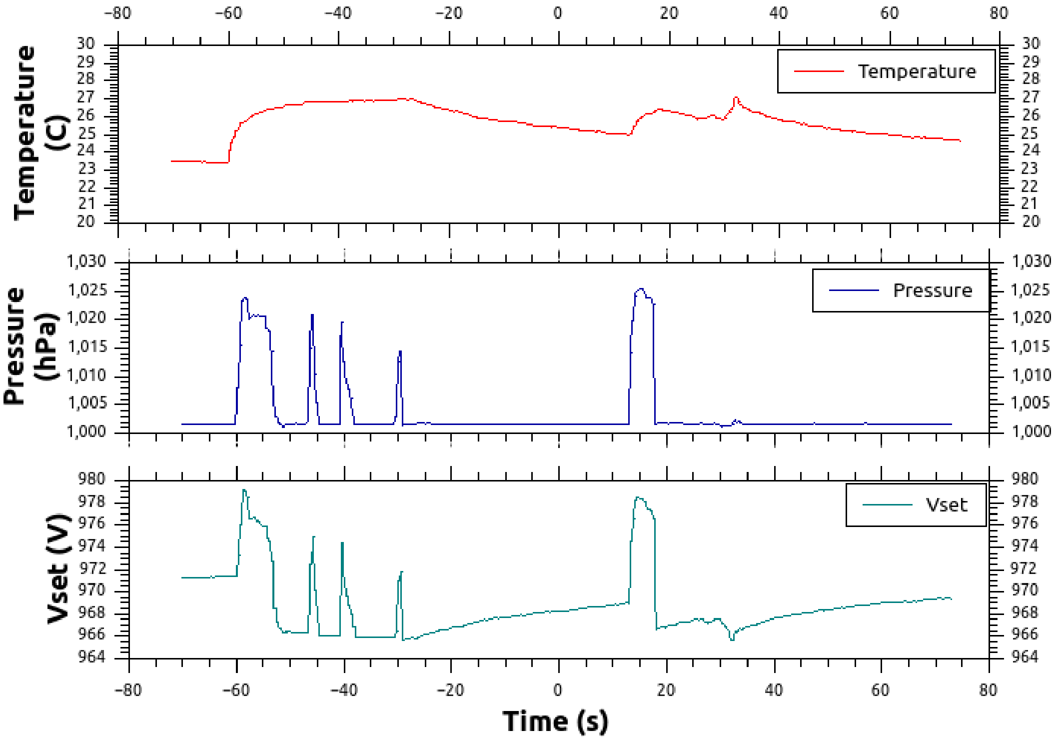


Figure 6.2: HV correction in function of temperature and pressure using Eq. 4.17.

These plots show the voltage correction (V$_{set}$) as a function of the pressure and temperature variations during a two minutes window. The operating system (FreeRTOS) running in the μP has a dedicated task that performs: the PT IIC transaction to read the data from the sensors, perform a pressure correction based on the temperature, calculate the corrected V$_{set}$, translate the value to DAC units and send it to the FPGA to set the HV.

The system is able to do pressure and temperature correction on the HV every 140 ms. Fig. 6.3 shows the PT voltage compensation (V$_{set}$) for Eq. 4.17 used for the HVPSS, and its corresponding measured output voltage (V$_{out}$). This automatic compensation feature can be enabled on-demand as a service provided by the system.

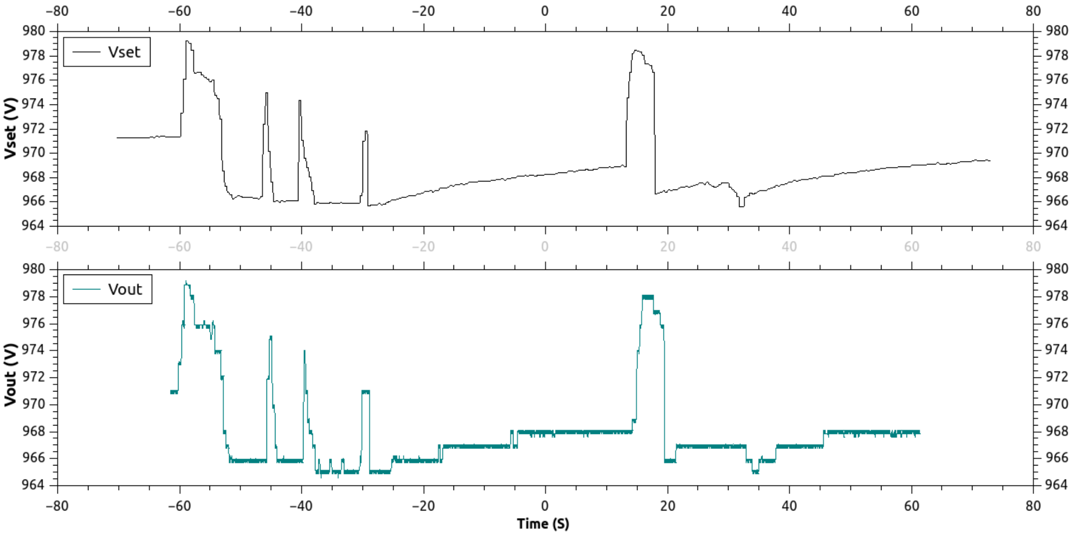


Figure 6.3: PT corrected voltage (V$_{set}$) compared with the output voltage (V$_{out}$) of the power supply measured with a HV probe.

6.1.2 Resolution Increase by Oversampling

At firmware level, it can be say that the DAQ for WCD system is a reduced version of the HVPSS. The framework architecture described in Chapter 4 gives to the system flexibility to implement any of both applications without much effort. The use of the ComBlock allows to reuse the RTL blocks from one system to another.

The common elements of external hardware in both systems imply that their controller blocks are the same. Many components of the timing distribution and signal analysis are common as well. Among these blocks, the most interesting result is given by the decimation block.

The sampling frequency of the ADC allows to detect and capture fast events with high resolution in time. The FPGA architecture allows doing in parallel decimation by oversampling to increase the resolution of the acquired data. This process allows to integrate the signal over N samples increasing the SNR by a factor $\sqrt{N}$ at cost of a reduction of the effective conversion frequency. The theory behind this process is explained in Section 4.1.4.

To test the decimation block, several measurements of current were digitized with the ADC ensuring a full-scale range of 30.6 nA. The decimation factor (N) was increased and the process repeated obtaining the experimental statistical error σ over 32.000 samples per measurement. The results of these experiment are shown in Table 6.1.

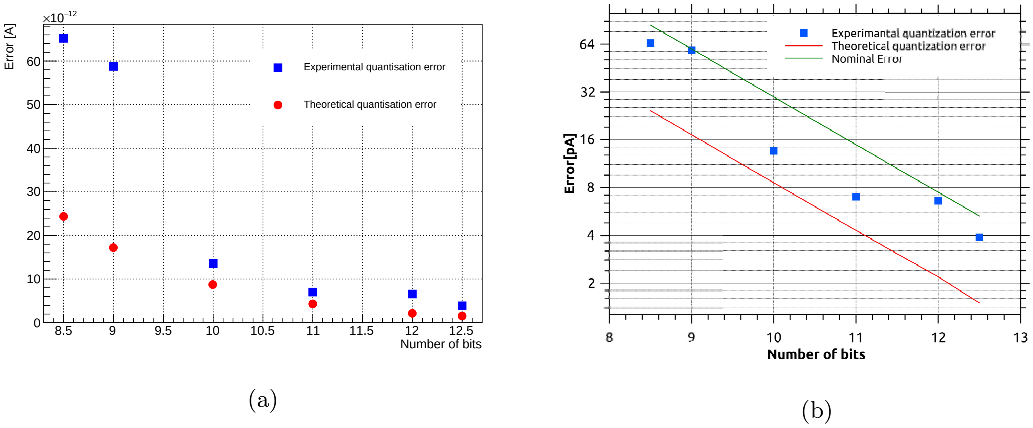
Table 6.1: Measurement of the current: effective number of bits (n_b), effective sample rate and nominal resolution error ($Delta$) versus the decimation factor. The ADC digitized full scale range of 30.6 nA with 8 bits of resolution and a nominal sampling frequency of 500 MHz

N	**ENOB** $\mathbf{n}_b$	**Effective Sample Rate (MHz)**	**Nominal Resolution** Δ **(pA)**	**Quantisation Error** $\sqrt{\Delta^2/12}$ **(pA)**	**Experimental Statistical Error** σ **(pA)**
2	8.5	250.00	84.4	24.4	65.2
4	9	125.00	59.7	17.2	58.8
16	10	31.25	29.8	8.6	13.6
64	11	7.81	14.9	4.3	7.0
256	12	1.95	7.5	2.2	6.6
512	12.5	0.98	5.3	1.5	3.9

To validate the experimental results, the experimental statistical error of the signal (σ) after decimation must be less than the new nominal resolution (Δ) consequence of the increase of ENOB n_b (Eq. 4.7). However, this error cannot be less than the theoretical quantization error σ_p which is the square root of the quantization noise power (Eq. 4.8). These can be observed in Fig. 6.4.

As the decimation factor increases, the experimental error approaches the quantization error as shown in 6.4b. By changing the y axis to a logarithmic scale it is possible to appreciate how the experimental error is bounded between the nominal error and the quantization error as shown in Fig. 6.4a. Is worth mentioning that this is only possible if the noise distribution is approximately Gaussian which is verified by the Histogram block. A comparison between a good noise distribution vs a non-ideal is shown in Fig. 6.5.

Although the decimation results were related to the HVPSS, this block is also used in the context of the DAQ system. Fig. 6.6 shows a typical pulse coming from a PMT sampled with different decimation values over a 80 μs window. While the time of arrival can be measured with the signal with no decimation applied (Fig. 6.6a), the amplitude and baseline can be



(a)

(b)

Figure 6.4: Theoretical quantisation error and experimental statistical error versus n_b 6.4a. Experimental error bounded between nominal resolution and minimum quantization error 6.4b.

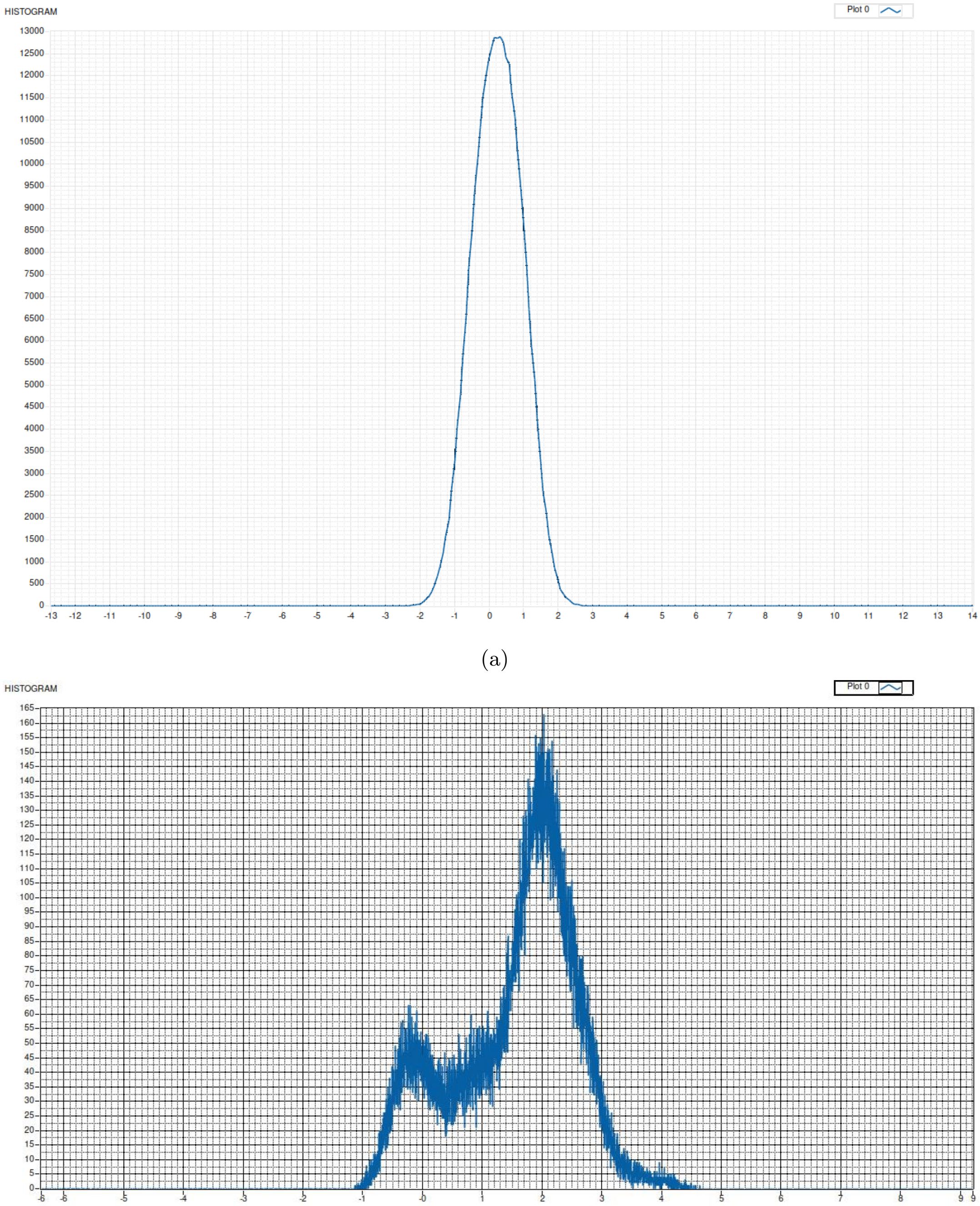
measured with more resolution using higher decimation factors (Fig. 6.6d and Fig. 6.6e).

The system is able to increase dynamically the maximum number of bits obtaining an experimental statistical error very close to the limit given by the quantisation error and bellow the nominal resolution (Fig. 6.4b). This is one of the strongest characteristics of the system allowing it to achieve measurements below 5 pA at effective sampling rate of 980 kHz. The tools provided by the system, such as the histogram allows to measure the quality of the noise to guarantee the integrity of the oversampling process. The benefits of the increased resolution are evident in Fig. 6.6 where the measurement of the peak of the pulse is critical to obtain the energy of the detector.

6.2 HVPSS for MPGDs Tests and Results

6.2.1 Picoammeter board calibration

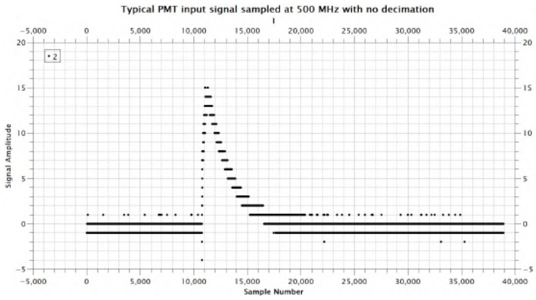
The linearity and noise analysis of different HV power supplies was discussed in Section 3.1.1 leading to the selection of the ISEG BPn4010512. The linearity and repeatability of the voltage and current monitoring (V$_{mon}$ and I$_{mon}$) respectively were also tested as shown in Fig 6.7. Both show a good linear response to different values of V$_{set}$ with a load resistor of 100 Ω. However, for low currents, the monitored current (I$_{mon}$) separates from the measured as shown in Fig.



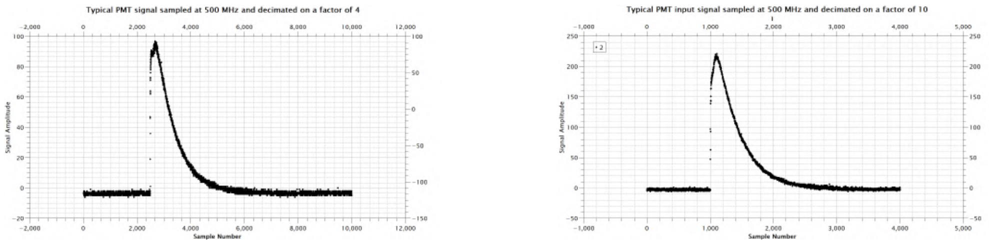
(a)

(b)

Figure 6.5: Histogram comparison between good noise distribution 6.5a and non-ideal noise distribution 6.5b.

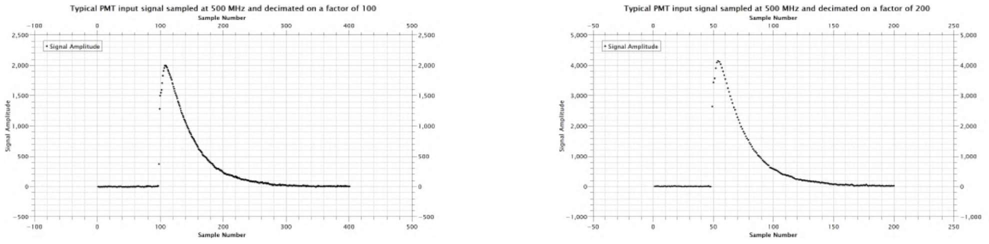


(a) No decimation, $T_s = 2ns$



(b) Decimation Factor of 4, $T_s = 8ns$

(c) Decimation Factor of 10, $T_s = 20ns$

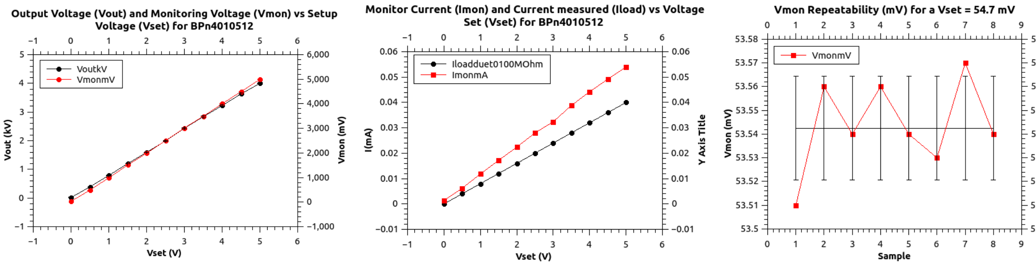


(d) Decimation Factor of 100, $T_s = 200ns$

(e) Decimation Factor of 200, $T_s = 400ns$

Figure 6.6: Typical PMT trace, captured at different decimation factors over the same window of time (80 μs.)

6.7b in contrast with the voltage monitored vs measured, as is shown in Fig. 6.7a. Both have good repeatability in the measurements with variations of less than 1 mV and non appreciable hysteresis as shown in Fig. 6.7c. This result is important because conducts to the decision to use the I$_{mon}$ readout for global current monitoring and stresses the importance of the picoammeter for precise current monitoring in the HVPSS for MPGDs. This is less significant for the DAQ for WCD because there is no need of high precision in the current monitoring of power supply.



(a)

(b)

(c)

Figure 6.7: Voltage monitoring (V$_{mon}$), Output voltage (V$_{out}$), Current monitoring (I$_{mon}$) and Current delivered (Iload) vs Set up Voltage (V$_{set}$) from the BPn4010512 (Figs. 6.7a and 6.7b). V$_{mon}$ repeatability for the same V$_{set}$ (Fig. 6.7c)

To calibrate the picoammeter board and ADC readout, the system is connected in series to a serial array of six 50GΩ (300 GΩ total) resistors and powered with the HV power supply. The Voltage until 500 V was measured with a Keytley 197A $5\frac{1}{2}$ digital resolution digital voltmeter [112]. Higher voltage measurements were done using a Lecroy PPE20kV HV probe. The current value is verified with a commercial Keytley 6485 picoammeter [113] connected in series with the system. The value of the resistor was also experimentally verified resulting in a value of $(298 \pm 2)G\Omega$.

The calibration of the picoammeter board for static input current has been performed to test the effects of impedance matching in the linearity of the picoammeter board. Fig. 6.8 is shown the ADC calibration for static input current measured at a sampling frequency of 2.6 kHz. The system linearity is not affected and there is no evidence of digital noise effects.

Fig. 6.9 shows the measurement of currents near to zero. The plot in Fig. 6.9a shows that the linearity holds even at lower currents. The box plot in Fig. 6.9b depicts the error deviation for 32.000 samples of different voltages obtaining a maximum deviation of 20 pA.

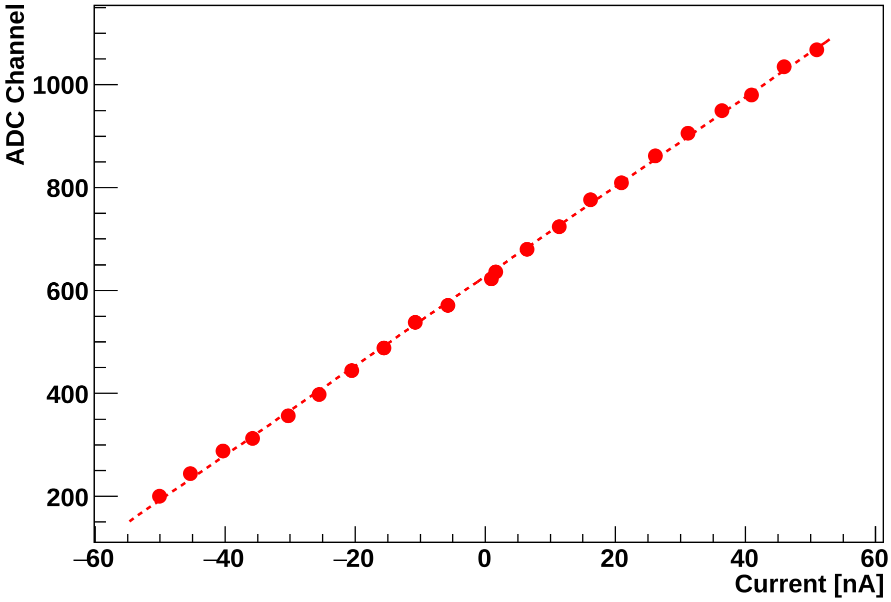


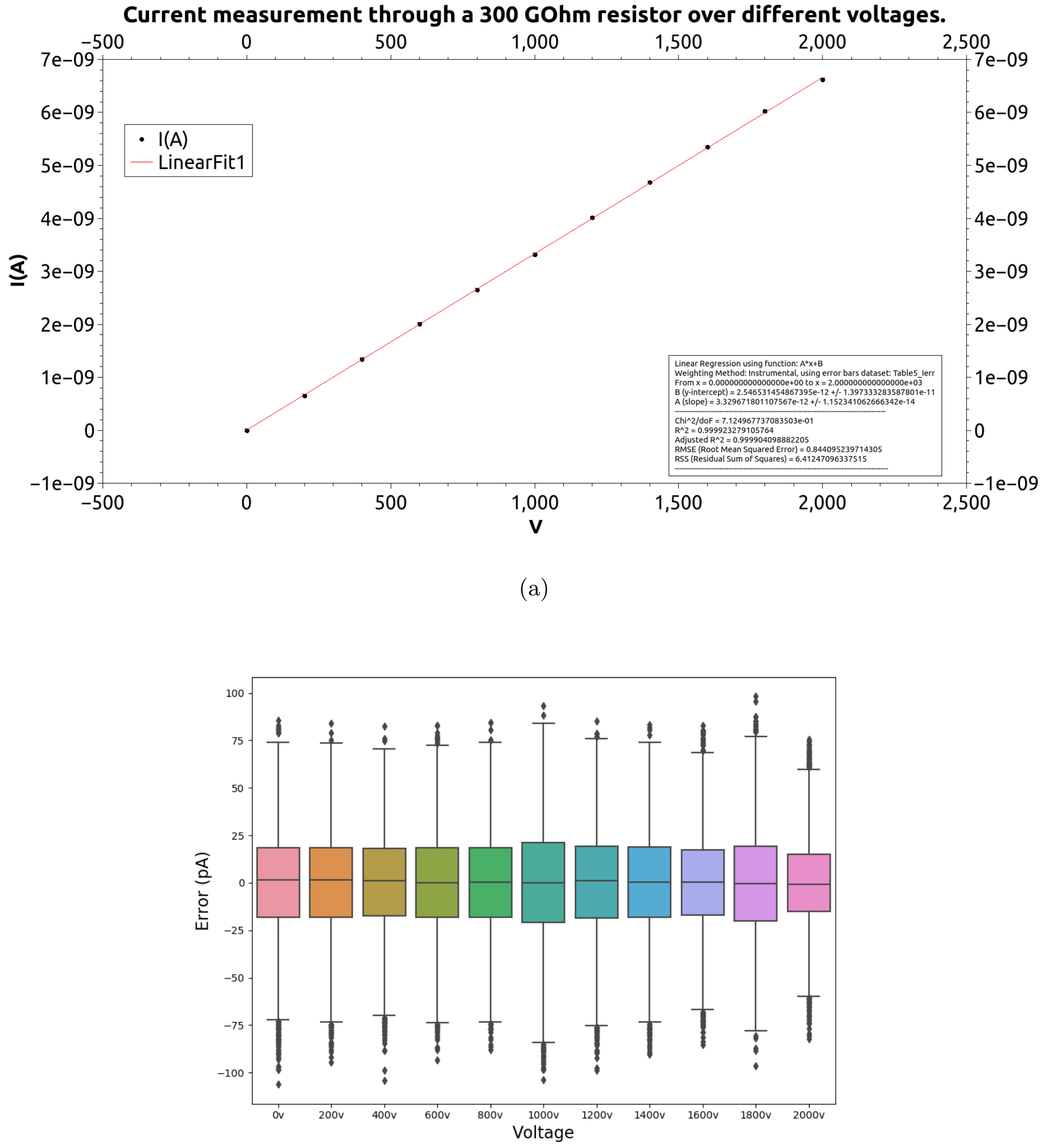
Figure 6.8: Calibration of the ADC board hosting the ADC08500 and the picoammeter board for static input current in the ±50 nA range

The symmetrical distribution of the noise is ideal for an increase of resolution by decimation. The system was able to achieve a 3.9 pA resolution with sampling frequency $\approx$ 1 MHz by applying a decimation factor N=512, as shown in the results of Table 6.1.

6.2.2 HVPSS Performance in a Test Beam Exercise.

In October 2018, a fully assembled prototype of a HVPSS channel (Fig. 6.10) was tested during a test beam exercise at the CERN SPS H4 beam line. The system operated for nearly two weeks powering one of the electrodes of the MPGD hybrid design. Specifically the MicroMegas mesh of the last multiplication stage in the hybrid mini-pad prototype (Fig. 2.8).

During the two weeks of operation, the system recorded the current provided to the micromesh at a sampling rate of 156 Hz. Several discharge events were identified and sampled at 500 Mhz storing a trace. One trace of current vs time as measured by the HVPSS is shown in Fig. 6.11. This data was collected during different beam setting conditions and different



```
Linear Regression using function: A*x+B
Weighting Method: Instrumental, using error bars dataset: Table5_Ierr
From x = 0.000000000000000e+00 to x = 2.000000000000000e+03
B (y-intercept) = 2.546531454867395e-12 +/- 1.397333283587801e-11
A (slope) = 3.329671801107567e-12 +/- 1.152341062666342e-14
--------------------------------------------------------------------------------
Chi^2/doF = 7.124967737083503e-01
R^2 = 0.999923279105764
Adjusted R^2 = 0.999904098882205
RMSE (Root Mean Squared Error) = 0.844095239714305
RSS (Residual Sum of Squares) = 6.41247096337515
--------------------------------------------------------------------------------
```

(a)

(b)

Figure 6.9: Current measurement over different voltages with a resistor load of 300 GΩ 6.9a and error deviation over 32.000 samples of each voltage 6.9b

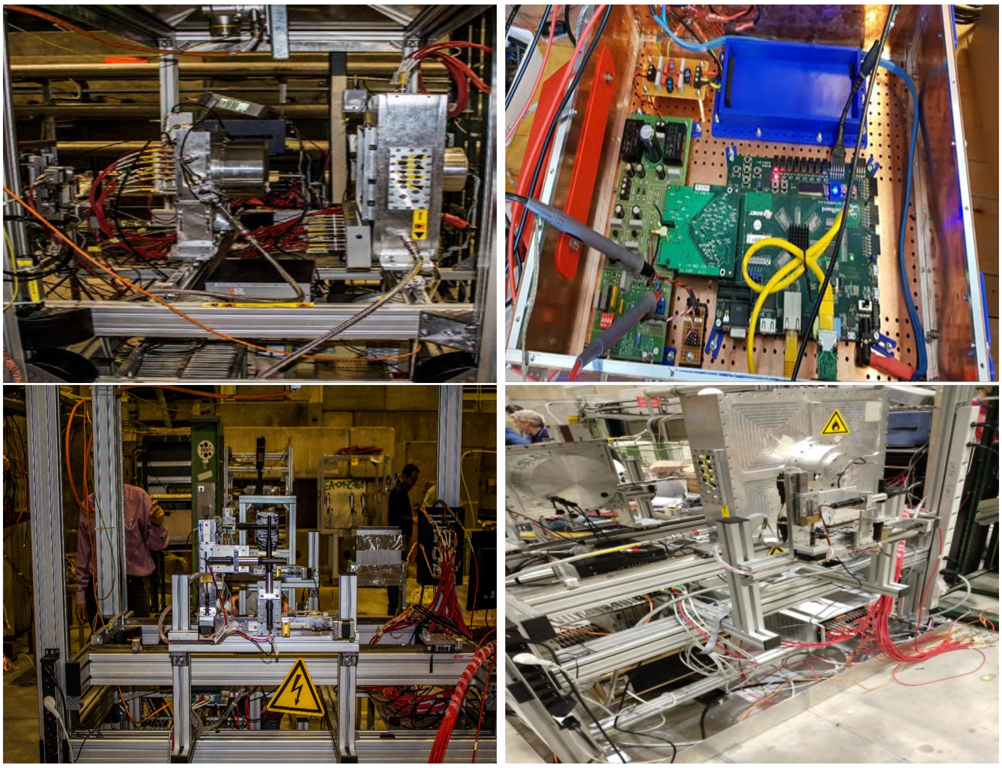


Figure 6.10: Experimental Setup in CERN SPS H4 beam line, October 2018

detector working parameters. The areas in the three rectangles highlight the different beam duty cycles, dotted lines marked the changes in the beam intensity (b.i.) and the dashed lines mark the changes in the detector gain (d.g.). The two dashed rectangles correspond to a high current surge related to detector discharges.

During the measurement period, the detector was subjected to different beam settings conditions. In Fig. 6.12 is shown a zoomed data sample of the variation in the duty cycle experienced by the detector.

As described in Chapter 4 the electrical discharges are handled in parallel and sampled at a 500 MHz sampling rate. The absolute timestamp of the event is generated when the high surge condition is detected. The first iteration of the HVPSS stored the electrical discharge in a FIFO.

An example of the parallel acquisition is shown in Fig. 6.13. The current vs time plot is shown on the left. The black dots represent the electrical discharges events. The figure at

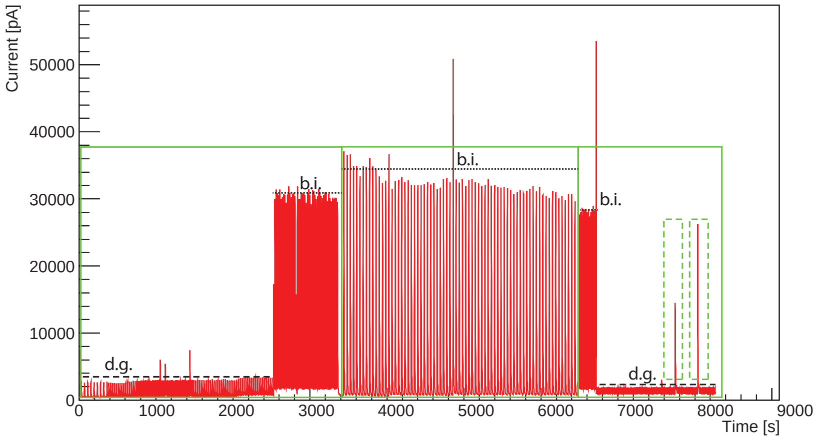


Figure 6.11: Current versus time as measured by the HVPSS during test beam exercise.

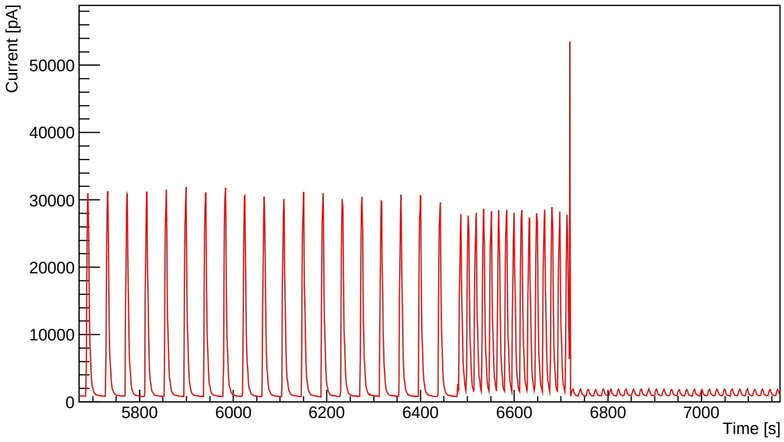


Figure 6.12: A zoomed view of a portion of Fig. 6.11. The variation of the beam duty cycle and of its intensity can be clearly appreciated.

right, the 500 MHz waveforms collected for the third discharge event. The time interval for the waveform collection is defined by the Samples Before Event (SBE) and Sample After Event (SAE) that limit the time range around the event time. Their value can be changed providing high flexibility in selecting the time interval of interest.

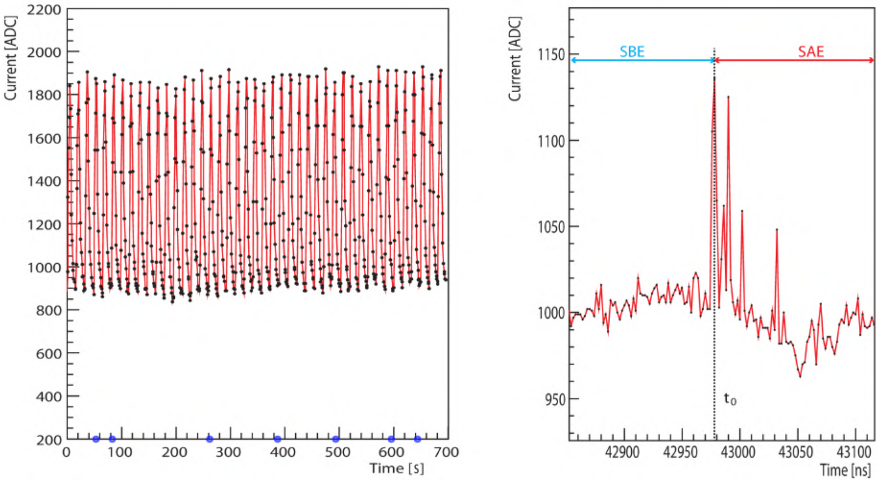


Figure 6.13: Measured current versus time. Left: the black dots are the measurements obtained applying the n factor, the read line interpolates them, the open blue circles mark the high surge current events. Right: the 500 MHz waveform is collected for the third high surge current event in the left plot.

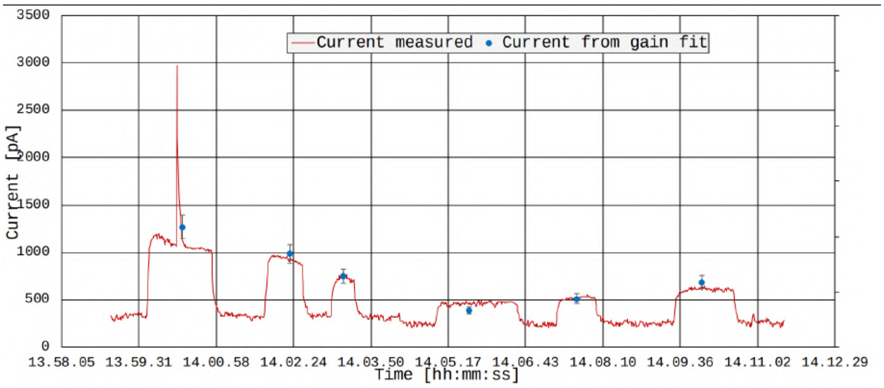


Figure 6.14: Cross check analysis from current measurement by the HVPSS and the current fit from the information of the detector.

A cross-check from the current measurement of the HVPSS was perform using the information gathered by the detector using a characterized UV LED to generate a current. The current values were obtained from a gain fit base in Eq. 6.1 and the result is shown in Fig. 6.14,

$$G_{eff} = \frac{I_{meas}}{C \cdot Rate \cdot \#e^{-}} \tag{6.1}$$

where G_{eff} corresponds to the gain of the detector, I_{meas} is the current measured, C is the charge of the electron, $Rate$ is the rate of incoming particles and $\#e^{-}$ is the number of electrons produced.

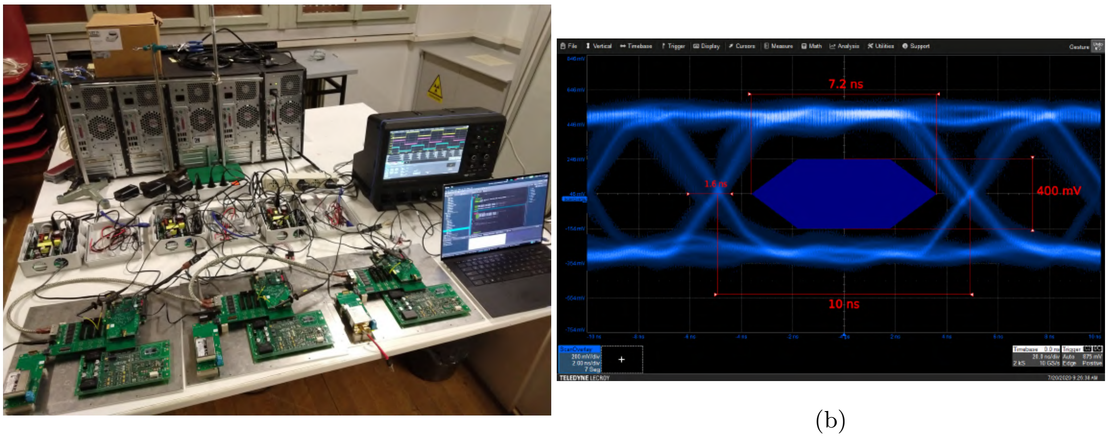
During the test beam at CERN, the system provided HV to one electrode of the MPGD. The system was able to do accurate current measurements under different beam and detector conditions, confirmed with the calculated current using the information of the detector's setup, as shown in Fig. 6.14. The HVPSS simultaneously detects, timestamps, and captures a trace of fast-transient events with 2 ns time resolution.

6.2.3 HVIBNI and Precise Time Synchronization Among HVPSS Channels

An experimental setup shown in Fig. 6.15a was built to test the dedicated communication network among three different channels using the HVIBNI. The setup consists of three HVPSS channels connected through a custom UTP cable covered with a tinned copper braid connected to the absolute ground. To measure the performance, the last channel is connected in series to a 20 GS/s oscilloscope Teledyne Lecroy Waverunner 8254 [114]. A data stream is generated from the farthest channel to measure any distortion effects. In multiple units connections operating at high-frequencies impedance matching should be considered to prevent or minimize disturbing reflections.

As mentioned in Section 3.1.4, the maximum transmission frequency is 100 MHz and must comply with the LVDS standard. An eye diagram was generated to measure the quality of the transmission (Fig. 6.15b).

With a transmission rate of 100 MHz, the HVIBNI keep an effective amplitude of 400 mV that is compliant with the swing range of the LVDS standard (from 250 mV to 450 mV). A maximum jitter of 1.6 ns and 7.2 ns of capture time complies with the ISO7821LLDW constraints [70]. The latency of voltage isolators discourage the use of the HVIBNI as a clock distribution channel. However, the implementation of a variation of the precise-time protocol (PTP) allows to synchronize multiple channels on the network.



(a)

(b)

Figure 6.15: Fig. 6.15a: Experimental of 3 HVPSS channels for HVIBNI testing. Fig. 6.15b: Eye diagram of data transmission at 100 MHz.

The VHDL block implementation and the modifications of the PTP were explained in Section 4.1.2. The synchronization process aims to measure the differences between the local clocks (Δ_n) with a master clock and correct it. To test the accuracy of the synchronization the experimental setup shown in Fig. 6.15 was used. The clock correction algorithm is monitored by the Xilinx Integrated Logical Analyzer (ILA) through a Digilent JTAG-HS2 module [115]. Each system provided a pulse-per-second (PPS) signal generated by the local clock and measured by a 20 GS/s LeCroy WaveRunner 8254 oscilloscope to observe the synchronization and measure the drift. A test framework (Fig. 6.16 was developed in the FPGA to measure the time synchronization under controlled conditions.

At power-up, each module has a different local time as shown in Fig. 6.17a. The master clock is represented in Channel 1 of the oscilloscope (yellow), the slave 1 is represented in channel 2 (red), and the slave 2 is represented in channel 3 (blue). All the modules will synchronize to the master clock. The synchronization routine will be initialized by the μP on the master HVPSS. After the Sync signal is sent to all the slaves, the result can be appreciated in Fig. 6.17b.

Despite the synchronization, the internal clock differences between the clocks can lead to a maximum drift of 200 microseconds in 24 hours as shown in Fig. 6.18. To compensate for the drift, a periodic sync signal need to be sent, to keep synchronization among the modules. Nevertheless, small "jumps" have been observed during the drifts and need to be further in-

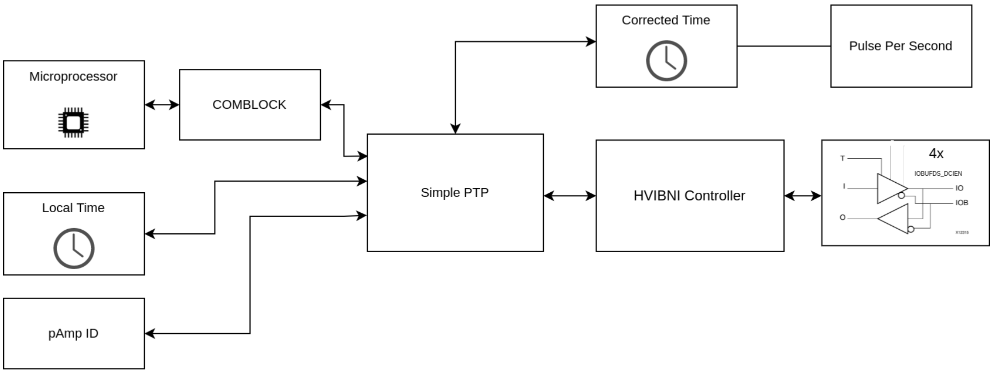


Figure 6.16: Block diagram of the test circuit implemented inside the FPGA.

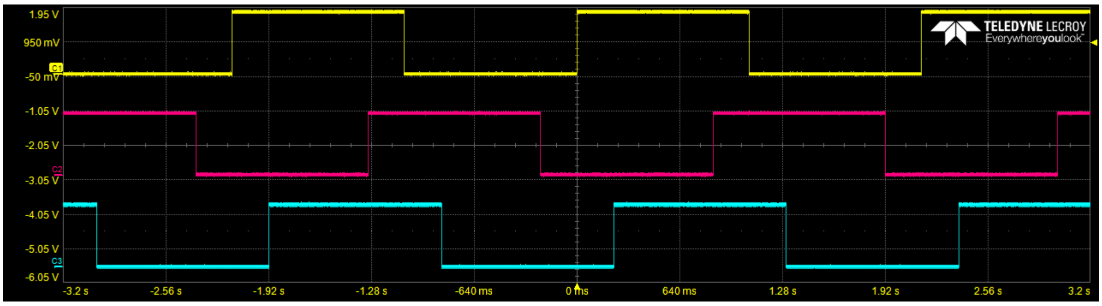
vestigated. Theoretically, the inherent error of the PTP synchronization is two clock cycles (8 ns at 250 MHz); however, experimental observations indicate an error of 20 ns. One of the causes may be related to small delays during the calculation of Δ_n (Equation (4.6)) plus the arithmetic operation to adjust the clock (Equation (4.1)) that may delay one or two extra clock cycles.

The HVIBNI provided a privileged network interface for the HVPSS channels to communicate among them with a maximum transmission rate of 100 Mbps and HV decoupling of 2000 V in continuous operation mode. The implementation of a simplified PTP algorithm on the FPGA allows to achieve time synchronization on several HVPSS channels with 20 ns error.

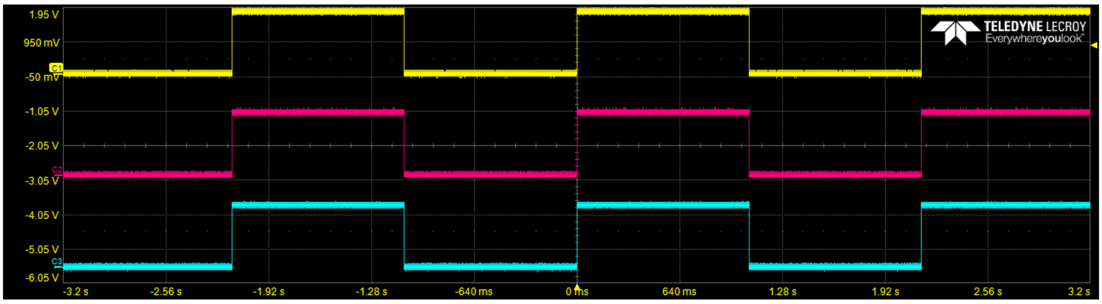
6.2.4 Multichannel HVPSS Test Exercise in RD51

In November 2021 a test exercise was performed in R&D collaboration laboratory RD51 at CERN. The aim of the test was to compare the HVPSS with a commercial CAEN N1471H power supply [116]. The experimental setup is shown in Fig. 6.19 consists in 6 HVPSS channels interconnected among them.

The detector used for the test is the COMPASS hybrid Minipdad prototype (Fig. 6.20). The chamber features two layers of THGEM in staggered configuration and a final MM multiplication stage. The total volume of the chamber is approximately 6 liters. A gas line connects to the detector with Ar:CO_2 70:30 line and both, input and output gas lines were connected to the output flow. Both THGEMs are divided into three sectors with a total of three "TOP" and three "BOTTOM" electrodes connected in series with a low-pass RC filter (1GΩ resistor and

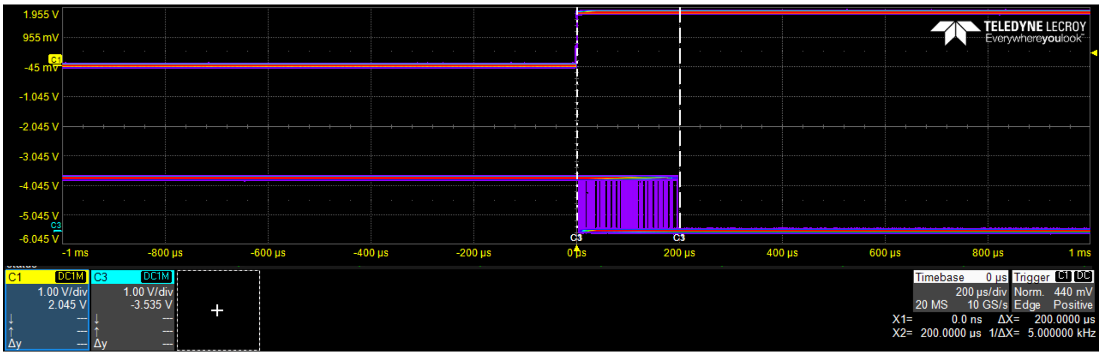


(a) PPS Signal before synchronization



(b) PPS Signal after synchronization

Figure 6.17: PPS signal before and after enabling the PTP synchronization routine.



C1 DC1M 1.00 V/div 2.045 V

C3 DC1M 1.00 V/div -3.535 V

Timebase 0 µs 200 µs/div 20 MS 10 GS/s

Trigger C1 DC Norm. 440 mV Edge Positive

X1= 0.0 ns ΔX= 200.0000 µs

X2= 200.0000 µs 1/ΔX= 5.000000 kHz

Figure 6.18: Time drift during synchronization

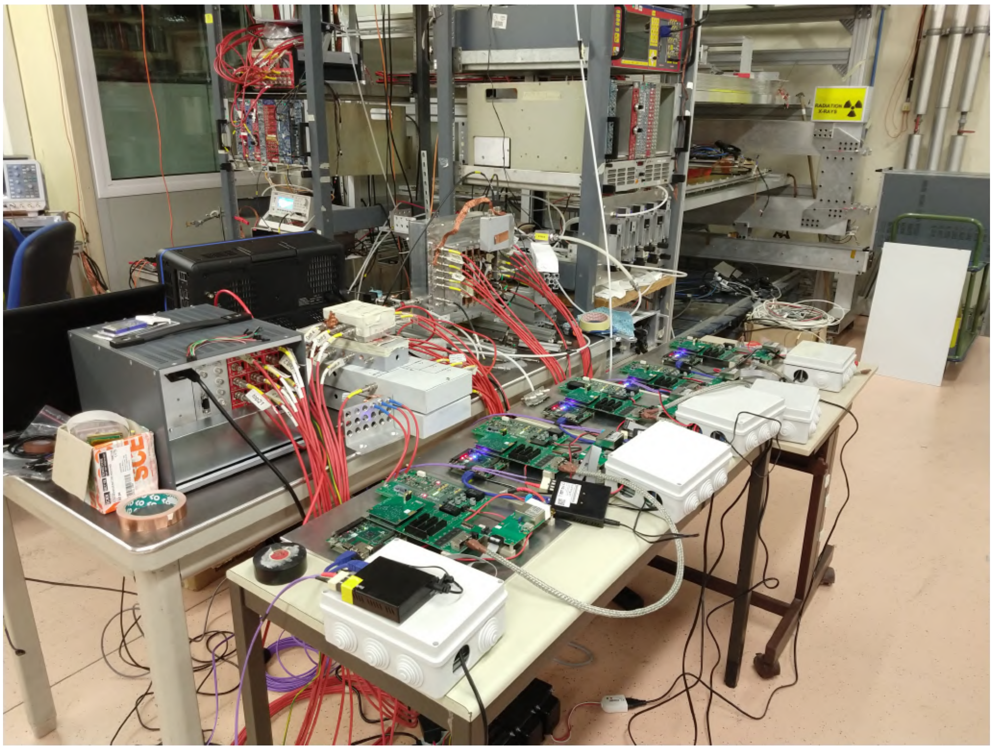


Figure 6.19: Multichannel test of HVPSS in RD51 laboratory at CERN, November 2021

22 μF capacitor). The electrodes are connected to the power supplies (PS) with the following configuration:

- The detector vessel is connected to the global ground.

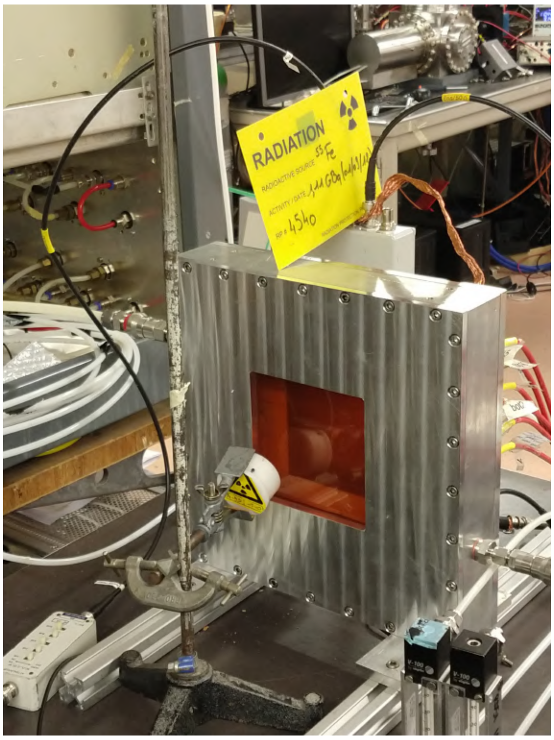
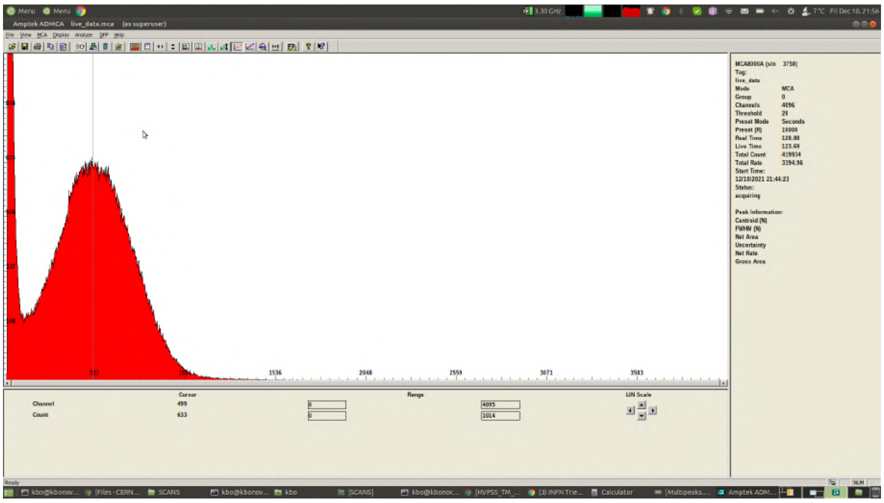


Figure 6.20: Minipad Hybrid MPGD prototype detector stimulated with ^{53}Fe source.

- The mesh is connected to the vessel through a 50 Ω resistor.
- The drift wires are connected to a PS in series to a low-pass filter (45.5 MHz cut frequency).
- The "TOP" electrodes are connected to a single PS.
- Each of the "BOTTOM" sectors of the THGEM are polarized by a single PS via a filtered distribution line.
- Each pad is decoupled from the others with a 1GΩ resistor, the voltage is distributed to the 1024 pads via 8 distribution boards (each hosting 128 resistors). The boards are connected in series with a 2 ns delay LEMO cables and power by 1 PS channel.

The charge is collected by a charge sensitive amplifier (CSA) (Cremat cr-110, G=1.4 mV/fC, rise time 7 ns, decay time constant 140 μs). The voltage signal was amplified and shaped by an Ortec 672 [117] with a shaping time of 3 μs. The output of the amplifier is fed into an

Amptek pocket multi-channel analyzer (MCA) 8000A to generate spectra. All the electronic readout chain has been calibrated injecting pulses of known amplitude into a 1pF capacitor connected to the input of the CSA. After taking the detector to operation conditions, all the sectors except the one used for the readout were disconnected. The detector is stimulated with a ^{55}Fe gammas source as shown in Fig. 6.21 illuminating the readout sector obtaining the energy spectrum shown in the figure.



MCA8000A (s/n 3758)
Tag:
live_data
Mode MCA
Group 0
Channels 4096
Threshold 21
Preset Mode Seconds
Preset (R) 10000
Real Time 128.88
Live Time 123.69
Total Count 419934
Total Rate 3394.96
Start Time:
12/10/2021 21:44:23
Status:
acquiring

Peak Information:
Centroid (N)
FWHM (N)
Net Area
Uncertainty
Net Rate
Gross Area

	Cursor		Range
Channel	499	0	4095
Count	633	0	1014

Figure 6.21: Spectrum of ^{53}Fe obtained from the MPGD polarized with the HVPSS.

Once the detector was set to stable operation the commercial power supply system was switched with the HVPSS. An estimation of the noise introduced by the power supplies (CAEN and HVPSS) and the picoammeter in different configurations respect to the filter was done (Fig. 6.22a). To estimate the noise several charges was injected in the electronics from 33 fC to 333 fC. The spectrum is obtained by the MCA extracting the centroid and the full width at half maximum (FWHM) value and the results are shown in Table 6.2.

There were no appreciable differences between the commercial power supply and the HVPSS in any configuration before the filters as shown in Fig. 6.22b where the respective plots of the spectrum overlaps. The last test was performed by connecting the picoammeter directly to the detector. As expected, the spectrum analysis shows a slight increase of the noise for both power supplies. A sample of the current measured was collected and analyzed in frequency (Fig. 6.22c) where immediately was noticed the contribution of the noise sources above the cut

Table 6.2: Noise effect in the detector comparison between CAEN N1471H module vs HVPSS.

	CAEN - FILTER		**CAEN - pAMMETER - FILTER**		**HVPSS - FILTER**		**HVPSS - pAMMETER - FILTER**	
Charge fC	**Centroid**	**FWHM**	**Centroid**	**FWHM**	**Centroid**	**FWHM**	**Centroid**	**FWHM**
33	311.58	6.64	311.43	6.56	311.59	6.28	311.57	6.38
66	627.45	6.61	627.32	6.59	627.62	6.22	627.48	6.36
166	1590.19	6.52	1590.01	6.56	1585.77	6.22	1591.2	6.28
266	2546.9	6.5	2548.83	6.5213	2543.31	6.31	2547.42	6.4
333	3184.85	6.57	3185.76	6.5	3182.18	6.34	3180.01	6.57

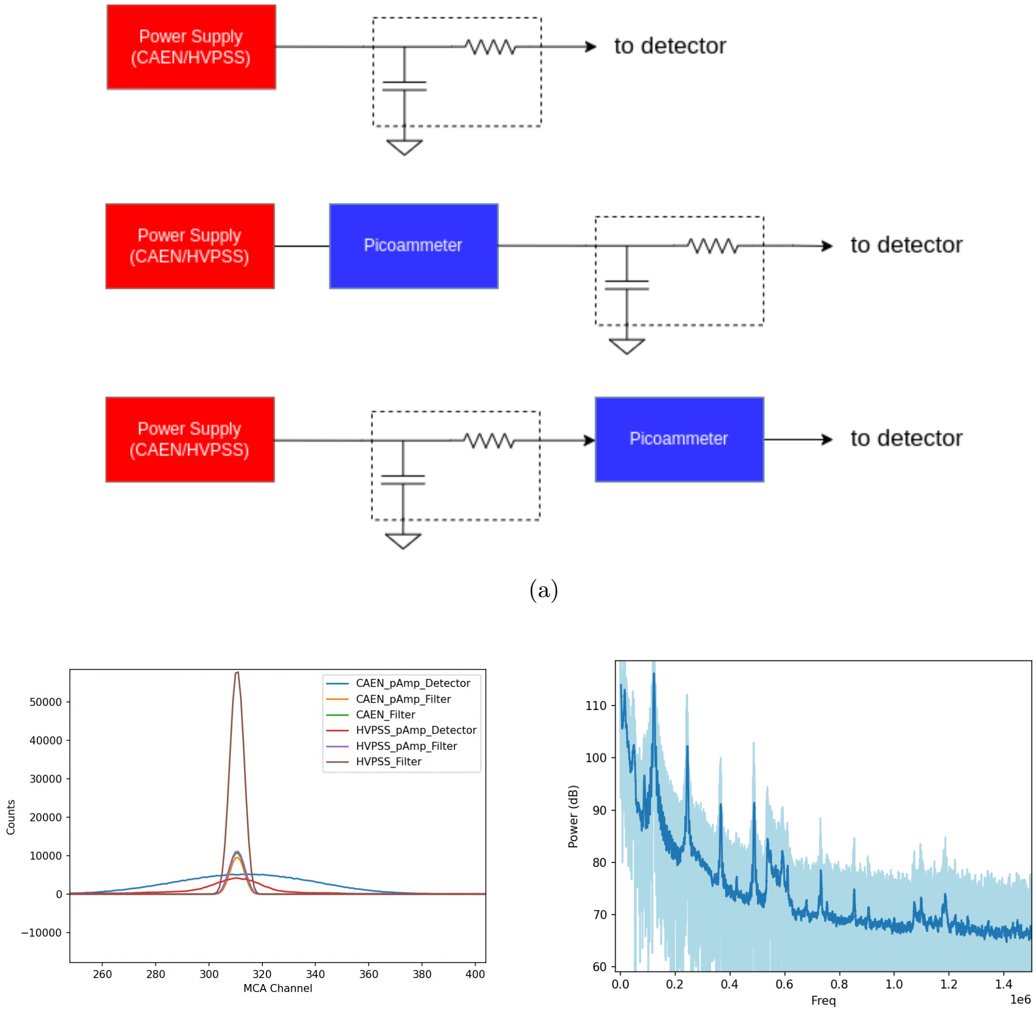
frequency of the filter (22 kHz).

It is worth observing that above 1.2 MHz there were not found significant noise sources and none of the electronics (including switching power supplies) used in the HVPSS works within these frequencies. If there is any noise contribution from the system, it will be a peak at 250 kHz produced by the readout clock output from the ADC. However, the lack of peak at 500 kHz (the closest is a well defined peak at 490 kHz) and other multiples of this frequency may discard this theory. Despite this, the noise contribution is within 5 pA keeping the HVPSS in range of the requirements of the system.

The study of the noise effect of the HVPSS to polarize the electrodes of the minipad showed an average FWHM error of 6.33 fC for a constant charge injection. There were no significant differences compared to the CAEN commercial power supply that showed an average error of 6.55 fC. Additionally, in contrast with the commercial power supplies, the tools provided by the HVPSS allowed to perform a noise analysis like the one in Fig. 6.22c.

6.3 DAQ for WCDs Tests and Results

Chapter 5 describes the modifications to the base system to be used as a DAQ for cosmic rays studies in WCDs. In Section 6.1.2 it was described the oversampling process to increase the resolution of a signal captured from a PMT (Fig. 6.6). This is ideal to analyze the energy of the pulses in a charge integration histogram like the one in Fig. 5.13a. This is a standard practice for cosmic rays studies and usually is done offline with the information extracted from the pulses (e.g. amplitude and rise time) however, in Chapter 5 was introduced the FIR-based PSD method for online classification. Two studies of PSD were performed during the research



(a)

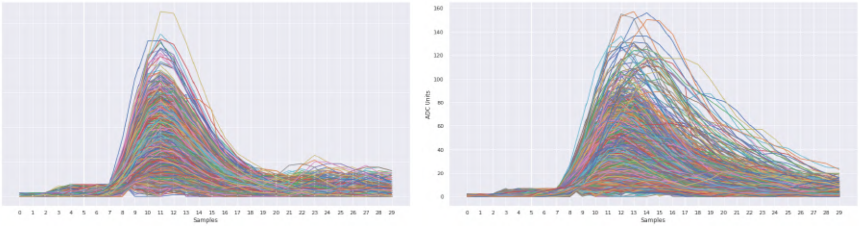
(b)

(c)

Figure 6.22: Noise analysis of different configurations of the power supply (6.22a) in the MPGD. 6.22b: MCA spectrum comparison for a 33 fC injected charge in the Detector. 6.22c: Noise Spectrum obtained from a current readout of the picoammeter system connected directly to the detector.

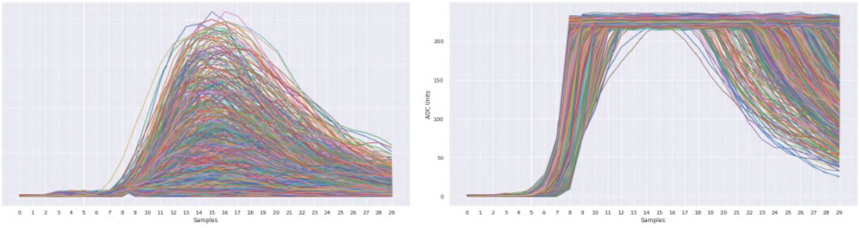
activity: muon-electron PSD, and PSD of three different types of particles obtained with the DAQ-WCD hardware, the results are described below.

The DAQ was used to collect pulses from the WCD experimental station for several days. These pulses were classified into clusters by its correlation distance. Fig. 6.23 shows three clusters with mayor contribution in the charge and one cluster with saturated pulses to exclude in the selection logic.



(a) Cluster 0

(b) Cluster 1



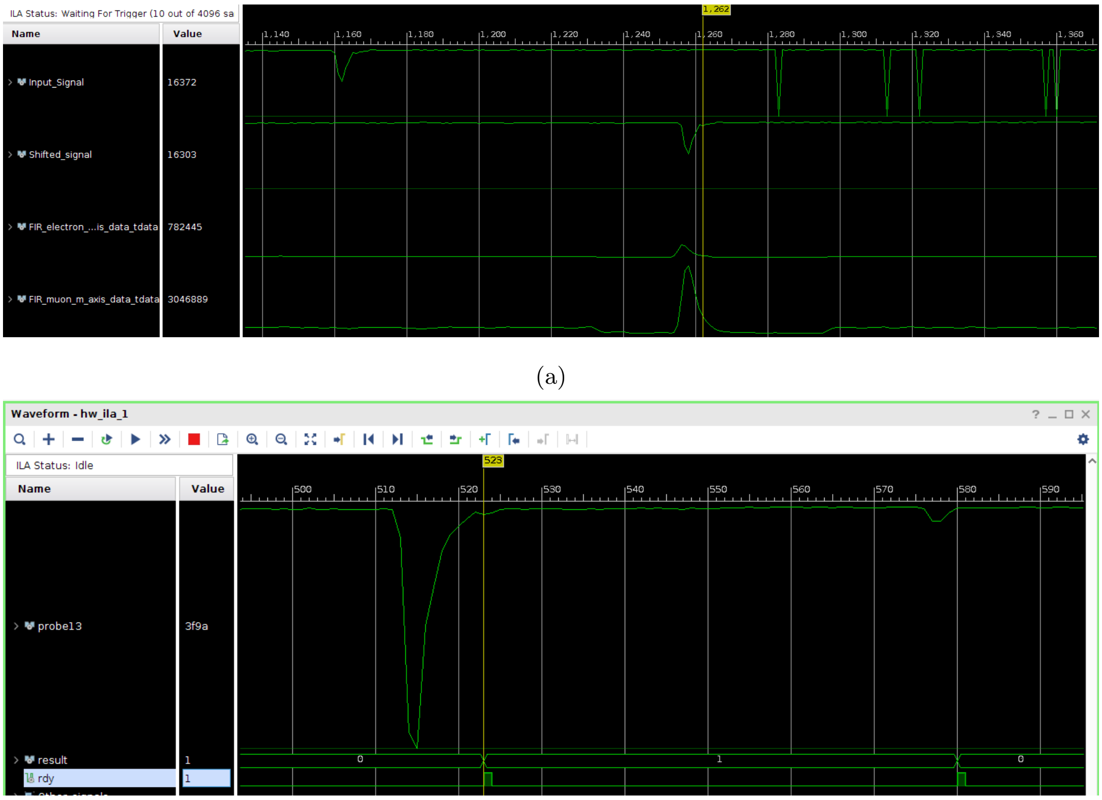
(c) Cluster 2

(d) Cluster 2a. (saturated)

Figure 6.23: Sample of raw pulse traces of each cluster

A representative pulse was selected based on the information from each cluster, obtained from there the coefficients for the FIR following the procedure described in Section 5.3. The correlation of the signal with each of the representative pulses is done in parallel with the result analyzed by the decision logic block. To visualize the process, the data stream is analyzed using Vivado's Integrated Logic Analyzer (ILA) as shown in Fig. 6.24.

In this example, the pulse is correlated with two representative pulses: one corresponding to a muon and the other to electrons. Fig. 6.24a shows the result of the correlation done by the FIR blocks ("FIR_electron" and "FIR_muon") for an input pulse. The "Shifted_signal" trace aligns the input signal to the point of maximum correlation. As it can be appreciated, the pulse has a higher correlation with the representative pulse of the muon than the electron. The



(a)

(b)

Figure 6.24: ILA capture of muon-electron correlation output from its corresponding FIR filters before the selection logic.

yellow line shows the point where the result is ready with a total output latency of 102 clock cycles after the pulse starts. Fig. 6.24b shows two consecutive pulses and the classification in real-time of a pulse type "1" corresponding to a muon and a type "2" corresponding to an electron. This configuration has a dead time of 1 clock cycle before it is ready to measure the next pulse.

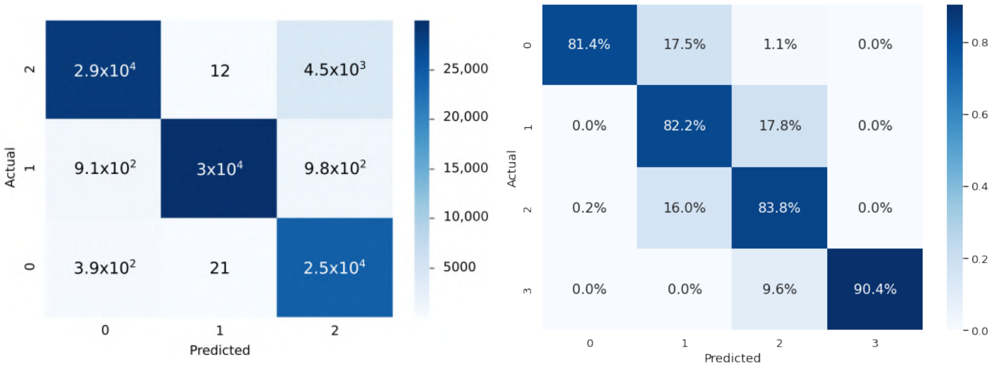
The FIR-based PSD block was tested for a ZC7Z020 Zynq SoC (Zedboard carrier), and in a ZU9EG Ultrascale+ (ZCU102 carrier). The reported utilization for a three particle identification is detailed in Table 6.3. The synthesis and implementation process was done in Vivado EDA design tool using the default configurations. It could be observed that the only significant resource utilization are the DSP blocks with 47% of utilization in the ZC7Z020 (Zedboard) compared in contrast with the 0% reported for the ZU9EG. This is related of the way that Vivado implements the FIR filters. By default the Zynq uses the DSP blocks to implement the FIR_Generator IP core while the Ultrascale+ uses a combination of look-up-tables and RAM blocks. This utilization can be further reduced by implementing more efficient FIR algorithms [118].

Table 6.3: Resource utilization comparison between XC7Z020 and ZU9EG

Platform	LUT	Registers	BRAM	DSP Blocks
XC7Z020	1.02%	2.00%	2.00%	47.7%
ZU9EG	0.20%	0.39%	0.39%	0.00%

The classification accuracy using FIR-based correlation for two and three pulse clusters is shown in Fig. 6.25. The FIR-based correlation was able to predict each particle with an overall accuracy of 92.5 % for the two-particle experiment, as shown in Fig. 6.25a, with a latency of 752 ns. For the three-particle experiment the overall accuracy was of 84.3%, as shown in Fig. 6.25b, with a latency of 224 ns. Both experiments were performed with a system clock of 250 MHz. By including an extra cluster, the overall accuracy was reduced in 8% without any significant impact in the latency.

Additionally, a classification algorithm based on ANNs was applied to the same data for two pulse clusters. The algorithm was executed on a CPU with AMD Ryzen 5, 8 GB RAM, Radeon Vega 8 Graphics, Ubuntu 18.04.5 LTS using Jupyter notebook and Python 3. In contrast with the FPGA implementation, the algorithm running on the PC obtained an overall accuracy of 96.62 % with an execution time of 44000 ns for each pulse in the two-particle experiment. These trade-off on overall accuracy (4%) for execution time (two orders of magnitude less) on a free-running DAQ allows to use the system as a powerful tool to save computational resources on post processing.



(a) PSD for two particles

(b) PSD for three particles

Figure 6.25: Classification accuracy representation in confusion matrices for a FIR-based correlation method for two and three particles.

Chapter 7

Conclusions

The objective of the applied research studies carried out through the three years of the doctorate program was to design and develop a multichannel high voltage power supply system (HVPSS) able to meet the specific requirements of a hybrid micropattern gaseous detector (MPGD) similar to the ones used on the RICH-1 detector in the COMPASS experiment. Several tests were conducted to select the proper components to build the modules comprising each HVPSS channel.

The first prototype of a single channel was tested under beam conditions at CERN. After analyzing the results obtained in the test beam, a new version of the HVPSS channel was built. This version included:

- Upgrades of the SoC-FPGA carrier.
- A redesigned high speed ADC and picoammeter boards.
- A new HV DC/DC supply board.
- A new interposer board with a HV network interface.
- A low voltage power supply system of each channel.

After the success of the tests with a single channel, seven more HVPSS units were produced. The multichannel system was tested by polarizing a sector of a hybrid MPGD and stimulating it with a nuclear source in the RD51 laboratory at CERN. Several tests were performed in the detector, including noise induction and stability, time synchronization, and network performance among HVPSS channels.

The designed system was able to meet the requirements needed to polarize a hybrid-MPGD, and the versatility of the design allowed to use it in the context of other types of particle detectors.

Every channel of the HVPSS provides a bias voltage in the range from 0 to -4 kV with steps of 61 mV. The system provides active pressure and temperature correction on the HV baseline each 140 ms to keep a stable gain on the MPGD. The voltage and current monitoring milestones were achieved, obtaining 15 mV of voltage monitoring resolution with a maximum frequency of 2 MHz.

The picoammeter precision was measured over 32.000 samples at different current values obtaining a maximum error deviation of 20 pA. The implementation of oversampling techniques increased the measurement's signal-to-noise ratio, reaching 3.9 pA of current monitoring resolution at a sampling frequency of 980 kHz exceeding the 10 pA required for the detector.

The system was tested under beam conditions polarizing one electrode of a hybrid-MPGD called minipad. The accuracy of the current measurement was corroborated by the data obtained from the detector in different configurations. The system captured fast transient events with 2 ns time resolution tested in diverse beam conditions.

Each HVPSS channel is galvanic decoupled and can be connected in cascade mode with other HVPSS channels. A dedicated high voltage isolated network interface (HVIBNI) was designed for communication among channels following a line interconnection topology. The HVIBNI consists of four bidirectional lanes with a maximum transmission frequency of 100 MHz and voltage isolation of 2 kV_{rms} in continuous mode and 8 kV maximum voltage for 15 minutes between neighbor channels. It achieved 20 ns of clock synchronization accuracy by implementing a modified precise-time protocol (PTP) through the HVIBNI.

The modular design of the HVPSS and the firmware based on the Open Source Framework Architecture (OSFA) in the SoC-FPGA allowed using the HVPSS channel also in the context of indirect measurement of cosmic rays as a Data Acquisition System (DAQ) of a Water Cherenkov Detector (WCD). The system was tested in a WCD experimental ground station to acquire pulses from cosmic rays. Each pulse was sampled and timestamped with 2 ns accuracy. The sampled data was used to implement pulse-shape discrimination algorithms in the FPGA for the online classification of particles produced by cosmic rays. A FIR-based correlation algorithm was designed to classify three types of particles obtaining an overall accuracy of 84.3% with a latency of 224 ns.

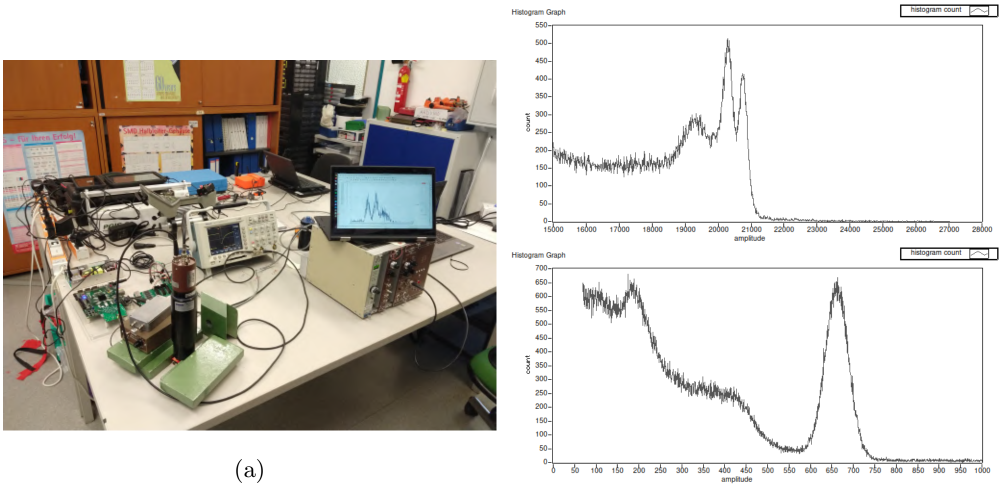
The HVPSS was able to meet the requirements to polarize a hybrid-MPGD. The modular design produced a scalable system to provide multiple HV channels. The specific needs of the detector lead to the development of custom hardware and advanced algorithms to achieve the required amplitude and timing resolution. The different HV power domains and the demanding timing constraints lead to the design of a HV isolated network interface and precise-time protocol algorithm to achieve nanosecond time synchronization on a galvanic decoupled system. The combination of these features produced a versatile instrument with characteristics not found in commercial devices.

Final Remarks and Future Works

Although the requirements for the hybrid MPGD were met, several tests can still be performed. A study of the propagation of electrical discharges can be conducted. Unfortunately, there was not enough time to do it during the research period. This study should be conducted under laboratory and beam conditions to find a correlation function to explain the fast transient phenomenon. The number of HVPSS channels was enough to polarize only one sector (six electrodes) of the MPGD. Further tests should be done by polarizing multiple sectors. Some minor issues like the mechanical placement of the different modules in the HVPSS channel may be considered in a new revision to improve the interconnection among them and reduce the occupation area.

The use of the system as a DAQ for cosmic rays studies can also be improved by adding an interface to connect two plastic scintillators for tracking vertical muons. Time over threshold algorithms can be implemented in the FPGA for precise measurement of the time-of-flight of the particle. Some improvements can be made in the FIR-based pulse-shape discrimination block to improve the accuracy, or eventually, this block can be replaced by a compressed artificial neural network.

Adding a digital pulse processor (DPP) block into the FPGA system to obtain the pulse amplitude combined with the decimation and histogram blocks already implemented can allow online spectroscopy on the DAQ. This feature is useful not only for cosmic rays studies but also



(a)

(b)

Figure 7.1: Experimental tests for nuclear spectroscopy using the DAQ system with a NaI scintillator for ^{60}Co and ^{137}Cs nuclear sources.

for nuclear spectroscopy. Some tests have already been conducted capturing pulses from a NaI scintillator with ^{60}Co and ^{137}Cs sources as shown in Fig. 7.1.

The HVPSS have been used to control the polarization of twenty five PMTs as a prototype of an electronic calorimeter (ECAL2), as shown in Fig. 7.2. These tests were performed as an exercise toward the Proton Radius Measurement (PRM) for the COMPASS++/AMBER experiment [119]. The final detector will comprise one hundred PMTs.

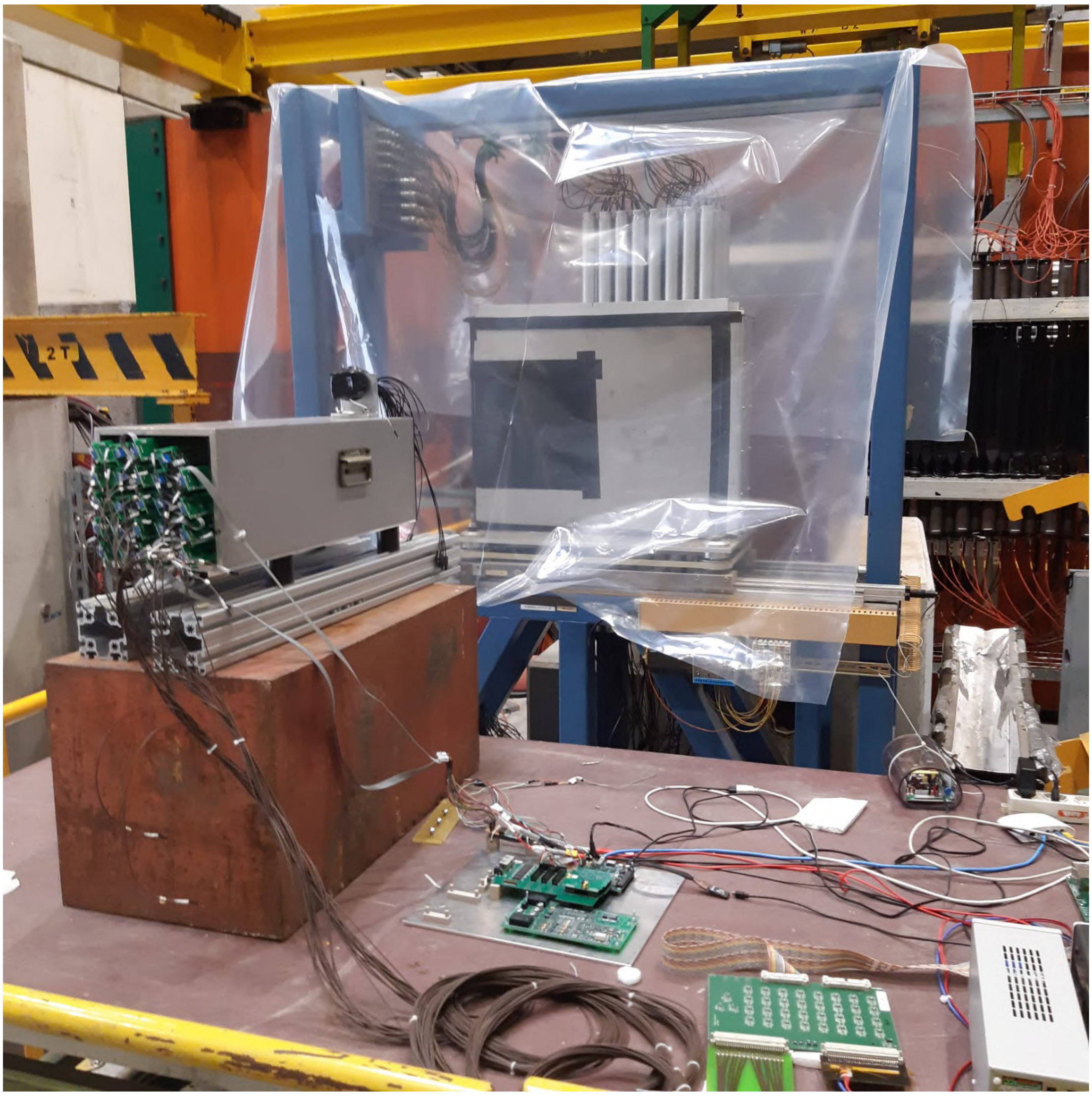


Figure 7.2: HVPSS used as voltage control to polarize 25 PMTs in an ECAL2 prototype in COMPASS M2 beam line, September 2021

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