High-Resolution Imager Based on Time-to-Space Conversion

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***Abstract*— We present a high-resolution 3-D (*X*,*Y*,*t*) imager for time-resolved experiments based on time-to-space conversion. The system uses cross delay line (CDL) detectors for particle identification and a fully configurable digital processor based on field programmable gate arrays (FPGAs) for 3-D image reconstruction. The instrument reaches a spatial resolution of 45 μm full width at half maximum (FWHM) (i.e., 18 μm rms) and a temporal precision of 15 ps rms. The detection rate achieved is 10 Mcps, with a dead time below 7 ns, leading to a global throughput up to 6 Gb/s. In addition to the state-of-the-art performance, the innovative aspect of the presented contribution resides in the complete reconfigurability of the instrument: it is, in fact, the first time that the time-to-digital converter (TDC) used for the time-to-space conversion has been fully implemented in programmable logic (PL), without the use of dedicated application-specific integrated circuit (ASIC) components. This advancement allows to adapt the instrument to the experimental setup without undergoing impractical hardware modifications.**

***Index Terms*— 3-D imaging, cross delay line (CDL) detectors, field programmable gate array (FPGA), free electron laser (FEL), synchrotron, time-resolved experiments, time-to-digital converter (TDC).**

I. Introduction

NOWADAYS, more and more experiments that investigate the dynamics of chemical, physical, and biological processes or the properties of atoms, molecules, and materials in general are based on techniques known as "time-resolved" [1], [2], [3], in which the collected measures combine information such as number, kind, and energy of the detected particles with their acquisition time. Many known and consolidated techniques in the study of matter such as (photo)electron spectroscopy [4] have seen, in recent years, their acquisition devices modified to obtain the additional temporal information.

This is particularly important in all the situations in which these techniques make use of instruments capable of generating pulsed light, such as lasers, free electron lasers (FELs,) or synchrotron radiation light sources [5]. In these cases, it is, in fact, possible to perform coincidence detection by combining different types of measurements, or "pump-and-probe" measures [6], which allow to reach temporal resolutions up to the femtosecond scale. Therefore, together with information about the energy and the emission angle of the electrons that are (photo)emitted by the sample under examination [7], [8], it is also possible to follow the dynamics of the occurring chemical–physical transformations [9], [10]. This analysis can be effectively and conveniently carried out on the condition that the detector is able to measure the times of occurrence of each characteristic event of the interaction phenomena. This type of detector must provide, for any single acquired particle (typically electrons, but sometimes also ions or photons), 2-D information with a spatial resolution in the order of, at least, a hundred microns, while also being capable of managing streams which, especially nowadays, with the advent of the third-generation synchrotron light machines, can be very large (in the order of several MCount/s) [11].

Today, the tools that allow to obtain measurements of time intervals with resolution in the picosecond scale are based on special electronic circuits called time-to-digital converters (TDCs) [12]. TDCs are traditionally implemented in application-specific integrated circuits (ASICs), such as the ACAM TDC-GPX device [13], and supported downstream by additional electronic resources, such as field programmable gate array (FPGA) [14], for real-time data elaboration. Nowadays, the enormous evolution of FPGA devices has unlocked the ability to obtain the same performance provided by ASICs [15], but with a fundamental difference: the latter provide virtually static characteristics and functional modes, while FPGA devices offer the total reconfigurability of the architectures implemented within them, allowing the same instrumentation to be optimized even for extremely different application needs [16].

Among all the detection methods that offer 2-D information, the most suitable for exploiting the TDCs' potentialities are based on cross delay lines (CDLs). As depicted in Fig. 1, these

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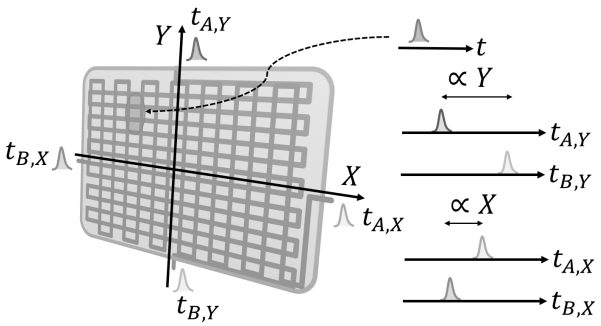


Fig. 1. Reconstruction of the planar position (X,Y) and temporal information (t) of a detected particle in a CDL. The spatial X and Y position are proportional to $t_{A,X} - t_{B,X}$ and $t_{A,Y} - t_{B,Y}$, while the t coordinate is proportional to the arrival time.

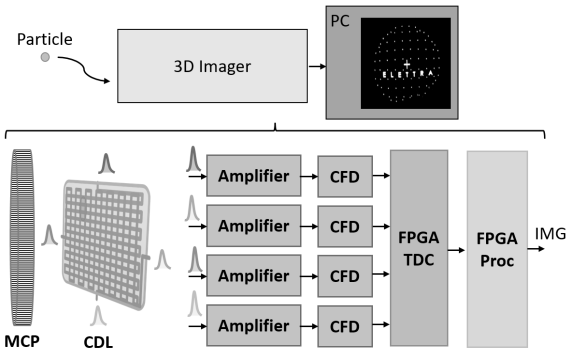


Fig. 2. Schematic of the presented imager.

detectors allow to reconstruct the information of the planar position (X,Y) of the interaction, time-to-space conversion, by measuring the different arrival times that the corresponding induced electric signal take to reach the ends of an array of lines. In addition, we can obtain the temporal information (t) by measuring the time distance between the electric pulses generated in the CDL detectors with respect to any external signal. CDLs find application in multiple research fields, from biological fluorescence imaging [17] to astronomy [16]. Although each individual section of the detector will be fully described later in this work, to understand the importance of a TDC electronics it is appropriate to anticipate a more detailed overview of how the detector works and of the stages that compose it (see Fig. 2). Each single particle (photon, ion, or electron) that reaches the detector is first transformed into a charge pulse by means of charge multipliers, typically consisting of microchannel plates (MCPs). Each single-pulse output by the MCP therefore determines an electromagnetic pulse on two 50-Ω matched CDLs (also called "meander lines") which propagates along the two directions of each of them [18]. At the end of the transmission lines, four amplifiers followed by constant fraction discriminators (CFDs) receive the pulses and generate digital pulses at their arrival; to be precise, thanks to CFDs, digital pulses are generated at the maximum of each analog pulse, which is why these detectors are also known as "centroid finding detectors." These digital pulses are sent to the TDC section, which measures and processes the arrival times of the pulses. Considering that the propagation along the delay lines takes about 1 ns to travel every mm, TDC electronics capable of resolving tens of picoseconds results in a detector capable of resolving tens of microns. This property, together with the ability to detect every single pulse (single-particle detector), makes these detectors much more appropriate than pixel-based systems in many applications, especially if time information is also required.

The purpose of this article is to present a state-of-the-art, innovative CDL-based imager entirely based on programmable logic (PL), i.e., FPGA, suited for time-resolved measurements, in particular for experiments that involve pulsed sources such as synchrotron radiation and (free electron) lasers. The proposed instrument reaches throughput up to 6 Gb/s, which traduce to up to 10 MCount/s on the CDLs, guaranteeing a spatial resolution of 45 μm full width at half maximum (FWHM) (i.e., 18 μm rms) and a temporal precision of 15 ps rms (i.e., 35 ps FWHM). The imager offers very good performance alongside a completely reconfigurable architecture, making it possible to properly tune both the TDC and the data processing system, thus achieving an enormous adaptability of the bundle to different, specific measurement setups and applications; this turns the proposed solution into a highly effective and complete research tool.

Fig. 2 shows a schematic view of the structure of the two FPGAs, one used as configurable TDC (FPGA TDC) and the other dedicated to fast data elaboration, image reconstruction, and data transfer through TCP/IP connection (FPGA Proc). The choice of such an architecture, where timestamp generation and image processing are performed by two separate FPGA devices, properly tunes not only the software but also, separately, the individual firmwares of the FPGAs to best fit with the requirements of the physical experiment.

After a short recap of the state-of-the-art (see Section II), a complete overview of the system and the description of the building blocks (i.e., CDL, analog-to-digital (A/D) interface, TDC, and processing of the image) are reported in Section III; in Section II are summarized the main contributions from the state-of-the-art. The experimental results are, then, presented in Section IV, and, finally, Section V covers the expected future developments.

II. State-of-the-Art

Recently, an exhaustive overview of performance characteristics of the main time-resolved detectors based on MCP with different readouts has been presented [19]. These kind of detectors convert each particle they receive at their input into a cloud of electrons that are, then, registered by proper detectors joined to the MCP. The CDL is just one out of many imaging architectures based on MCP. The most common of these architectures, when great temporal resolution is not required, consists in placing a phosphor screen behind the MCPs so that, when hit by the charge pulses, a light pulse is generated which is recorded by a charge-coupled device (CCD) camera. In [19], the authors comprehensively cover the state-of-the-art of many architectures, and in that work CDL detectors are highlighted to reach the best compromise between spatial resolution, up to 20 μm FWHM, and temporal precision, 10–100 ps rms.

TABLE I

SUMMARY OF THE STATE-OF-THE-ART

Feature	This work	[17]	[22]	[12]	[11]
Spatial resolution [μm FWHM]	45	40	25	87	105
Time precision [ps r.m.s.]	15	42.5	-	50	27
System type	TDC	TAC	TAC	TDC	TDC
Max. count-rate [kcps]	10,000	10	600	1000	1000
dead-time [ns]	7	1400	1667	-	10
Reconfigurability	YES	NO	NO	NO	NO

In these detectors, the time performance and spatial resolution are highly dependent on the performances of the used TDC. As a matter of fact, the TDC is the bridge between the physically observed phenomena and digital processing; this is why the main figures of merit of the global systems, e.g., resolution, dynamic-range, dead time, and count rate, are strongly related to the TDC architecture in use. This is the reason why detectors with high resolution are interfaced to an equally high-resolution time interval meter (e.g., TDC), to extract the timestamps without hampering its performance. CDLs made initially use another type of time interval meter, called time-to-amplitude converter (TAC) [20], which is capable of achieving excellent temporal (and therefore also spatial) resolutions with respect to a TDC solution of the same technological node [21]. While a TDC directly converts time events into a digital number, i.e., timestamp, in a very short amount of time (tens of nanoseconds), TACs convert a time interval into a voltage level which then needs to be digitized by means of A/D converter [22]. This aspect strongly limits the acquisition rate not higher than a few hundreds of kcps, and the event-to-event minimum needed time, dead time, on the order of several microseconds, which are not extremely high values.

Recently, the need of multihit acquisition has moved the researchers to look for a replacement to TACs in the CDL systems, thus opting for TDCs. This choice reduces the spatial resolution from a minimum of 10 μm FWHM down to 60 μm FWHM but allows a large increase to the count rate capabilities, going from hundreds of kCount/s up to some MCount/s, reducing the dead time from thousands to tens of nanoseconds. An overview of these solutions is reported in Table I, where the first column refers to the performances of the imager presented in the present article.

Nowadays, the standard architectures used for TDCs are ASIC. This makes very hard, if not straightforward, to modify the characteristics of the TDC (e.g., number of channels, resolution, dead time, and count rate) to adapt the acquisition system to specific requests, for example, by relaxing the resolution to increase the count rate and vice versa, unless hardware modification is made. For this reason, in this article we propose a complete configurable architecture with the state-of-the-art performance, where not only the data processing system but also the TDC are completely tunable firmware modules implemented on FPGA devices.

III. SYSTEM OVERVIEW

In this section, we give a more detailed description of the main elements that compose the imager. As anticipated in Section I and represented in Fig. 2, the system is composed by a CDL detector with an MCP used for charge multiplication (Fig. 3), an A/D front-end stage used to convert the analog pulses at the output of the meanders of the CDL into digital pulses (see Fig. 4), and a fully digital part consisting of two distinct FPGAs, a Xilinx 28-nm Artix-7 used for the TDC (FPGA-TDC), and an Intel 28-nm Cyclone V as system control and real-time data processing (FPGA-SCDP). Fig. 5 reports real images of the printed circuit boards (PCBs) of the FPGA-TDC and the FPGA-SCDP.

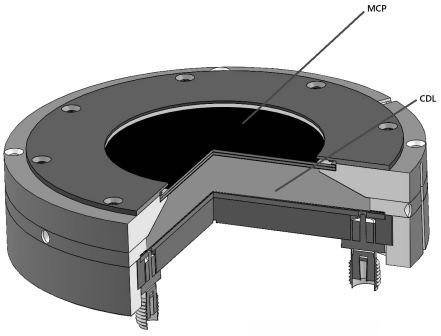


Fig. 3. MCP (top) connected to a CDL detector (bottom).

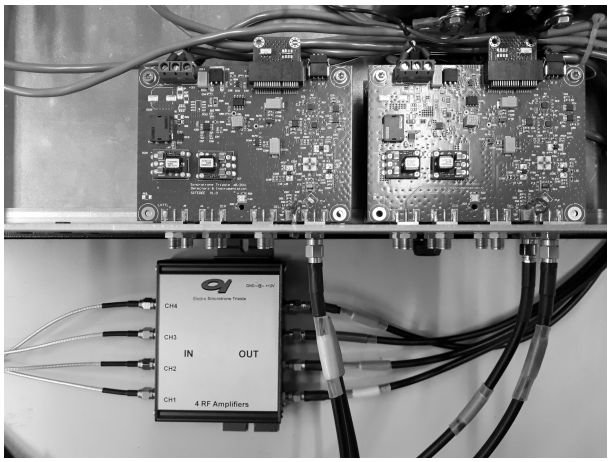


Fig. 4. A/D front-end composed by RF amplifiers (bottom) and CFDs that digitize the signal (top).

A personal computer is connected to the Intel 28-nm Cyclone V via 1 Gbit/s Ethernet link.

The A/D stage includes radio frequency (RF) amplifiers and CFDs, preserving the information of the arrival time of the pulses against their amplitude variations. The CFD outputs are sent to the FPGA-TDC, which determines the arrival time of the incoming pulses with respect to a reference signal, which can be either internal or external. The obtained timing information is then sent to the FPGA-SCDP, which performs system control and data processing tasks aimed to the real time-determination of (X,Y) coordinates and correlation to the related timestamps, to allow an easy reconstruction of 3-D images (X,Y,t). The FPGA-SCDP also manages the handshake of a user datagram protocol (UDP) communication protocol with the control and data acquisition PC.

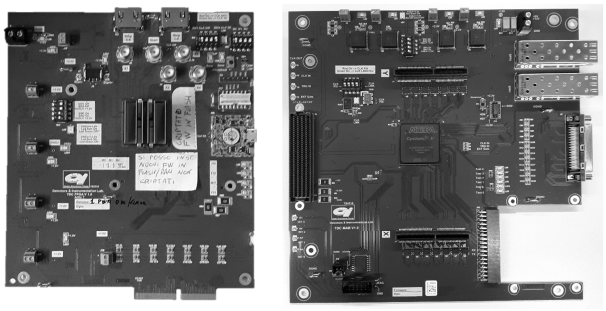


Fig. 5. PCBs used for the proposed system: FPGA-TDC with a Xilinx 28-nm Artix-7 FPGA used for the TDC (left) and FPGA-SCDP with Intel 28-nm Cyclone V FPGA used for system control and real-time data processing (right).

The proposed double-FPGA architecture is called the POLIMI-ELETTRA system, and it has been developed at four hands by the Politecnico di Milano (FPGA-TDC) and Elettra Sincrotrone di Trieste (CDL, A/D, and FPGA-SCDP). The present system comes as the evolution of a standard single-FPGA architecture, called THR02-TDC [11] developed by Elettra Sincrotrone di Trieste, where an ASIC, the ACAM TDC-GPX [13], was used as TDC. A great advantage of the FPGA-based TDC novelty is the intrinsic possibility of acquiring events uninterruptedly for very long periods of time, up to several hours, without any detrimental effect on the quality of the measurement. From this point of view, the POLIMI-ELETTRA system is extremely more versatile than the former TDC-GPX-based one (THR02-TDC), where a sensible deterioration of the time precision could already be observed for arrival times just beyond 1 μs. In addition, the absence of latencies that were previously required to periodically reset the TDC-GPX chip makes the new system very appealing whenever a continuous recording of events is required, for example, in long coincidence experiments. From the FPGA-TDC standpoint, the biggest effort is in the reduction in the minimum pulse-pair resolution, which is typically around 7 ns.

In the presented double-FPGA architecture (POLIMI-ELETTRA), the main innovative aspect of the instrument lies within the implementation of the TDC core in a fully customizable programmable device. The great flexibility of this approach allows to tune the performance, characteristics, and even the number of channels on the TDC while keeping the overall architecture untouched. In the following, we not only report the performance of the proposed POLIMI-ELETTRA system but also compare the two systems. In the next paragraphs of section III, an in-depth description of the various parts of the imager will be provided.

A. Cross Delay Line Detector

The CDL detectors provide reconstruction of bidimensional spatial images with high time resolution and count rate capability in addition to single-particle sensitivity. The detector structure (see Fig. 1) consists of two orthogonal 50-Ω transmission lines (meanders) placed behind a stack of MCPs. The MCPs convert the interaction of an impinging particle (e.g., electron, ion, photon) into a pulse charge that propagates from the position of generation toward both the ends of the corresponding lines of the arrays. Depending on the point of impact on the meander, the pulse will reach the two extremes at different times and, by calculating the time difference between the two events, spatial information ("X" and "Y") is extracted. The further estimation of the arrival time ("t") of the detected events returns a 3-D time-resolved information, which is the reason why these are sometime called 3-D (X,Y,t) detectors. In this sense, the imager can be thought of as a camera that records a sequence of 2-D frames over time.

B. Analog-to-Digital Front-End

The electromagnetic pulses generated by the CDL have an amplitude of few millivolts, and therefore, a proper conditional stage is mandatory, as shown in Fig. 2. At the extremity of each of the two anode lines of the CDL detector is placed an RF amplifier followed by a CFD that converts the analog pulse into a digital one, compatible with the low-voltage differential signaling (LVDS) logical input standard of the TDC. Since the meander lines are transmission lines with a characteristic impedance of 50-Ω, RF amplifiers with matched inputs are the preferred choice to amplify the signals and they are mounted close to the detector to reduce the likelihood of interference with external noise sources. The shape of the pulses is Gaussian, with FWHM equal to 4 ns, and rise and fall time around 2.8 ns, meaning that the signal energy lies in a bandwidth below 150 MHz. Given those specifications, each amplifier consists of the cascade of two GALI-S66+, monolithic microwave integrated circuits (MMICs) produced by minicircuits [23]. The overall gain is about 43 dB from 100 kHz to 1 GHz (cut-off frequencies at -3 dB), with a flatness of $+/-0.5$ dB from 1 to 400 MHz. Matching is guaranteed by $S11$ and $S22$ better than -20 dB and noise figure lower than 2.5 dB at 300 kHz, both in the band of interest. The output of each RF amplifier is connected to the input of a CFD which converts analog pulses (now amplified with an amplitude that varies between 0.5 and 2 V) into digital signals (compatible with the logical input standard of the TDC, i.e., LVDS) by extracting the time position of the peak of the Gaussian input signal regardless of its possible amplitude variations. In fact, the pulses generated by the MCPs placed above the two orthogonal anodes in the CDL detector have variable amplitudes according to the working voltage of the MCPs and the count rate of the events. This makes it impossible to use simpler solutions for digital conversion of the arrival time information of an event, such as common threshold discriminators with proper rejection of the walk error [24]. The presence of a transformer at the input of the CFD makes it easily adjustable for operation with positive or negative pulses. As well-known, the presence of noise and pulse amplitude variations at the input of the CFD might introduce a temporal uncertainty in the digital output. An adjustment circuit for compensating this effect is present in the CFD architecture. The experimental evaluation confirmed that the uncertainty of the CFD digital output below is 17 ps and around 9 ps FWHM, regarding jitter and walk error, respectively.

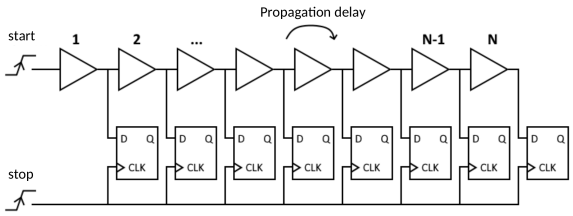


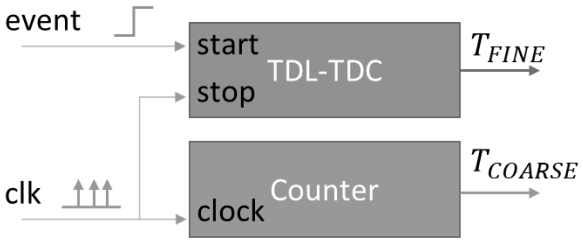
Fig. 6. Principle structure of the TDL-TDC.

C. FPGA-Based TDC

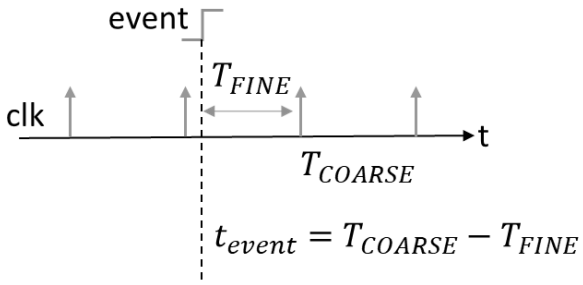
The timestamps are provided by a tapped delay-line-based TDC (TDL-TDC) [25] with resolution (LSB) of 2.17 ps over a full-scale range (FSR) of 0.145 ms, single-shot channel precision below 12 ps rms, minimum dead time of 7 ns, and an integral nonlinearity (INL) error lower than 4 ps over a dynamic range of 500 ns. These features are able to match the performance in terms of final image reconstruction of available systems currently in the state-of-the-art. The performance of the implemented TDC is summarized in Table II.

In principle, the TDL-TDC consists of a chain of buffers (bins or taps) that are used as delay cells in a delay line, and the measurement of time is performed by counting the number of bins passed through by the signal between the "start" and the "stop" of the measure. Basically, the TDL-TDC consists of a chain of buffers with outputs registered by flip-flops. In this sense, the TDL converts the interval limited by the couple of time markers "start" and "stop" into a number. Operationally, the "start" event, which is simply a binary transition, is propagated along the buffer sequence, whose outputs are the inputs of the flip-flops. The flip-flops clock gate (CLK) is the line where the "stop" marker, ending the interval, occurs. On the "stop" signal, the flip-flop chain simultaneously captures the output status of all the buffers, returning as output (Q) a sequence of 1 s of length proportional to the duration of the time interval under measure. This thermometric code form of the measurement value is, then, finally decoded into binary format (see Fig. 6).

In this architecture, the resolution of TDC is dependent on the propagation delay of the buffers constituting the delay line. In these terms, the performance of this basic architecture would be unacceptable mainly due to two aspects: it is limited, on one hand, by the propagation delay of the bins of the FPGA device (tens of picoseconds for the 28-nm) and, on the other hand, by the mismatches of the propagation times through different buffers (up to 3 to 4 times the mean propagation delay), which is also due to their pattern of layout [25]. These unavoidable problems related to the structure of the device have negative impact on resolution and linearity, which require to be addressed using specific techniques of subinterpolation and calibration [26]. More precisely, the subinterpolation compensates for the lack of native resolution (achieving an LSB of units of picoseconds for the 28-nm), while the calibration allows the system to recover excellent linearity. Moreover, the use of the Nutt interpolation technique [27] allows the implemented TDL-TDC to achieve a dynamic range extended to over 10 s also working in synergy with a digital counter



(a)



(b)

Fig. 7. Principle of the Nutt interpolation on a TDL-TDC. (a) Architectural overview. (b) Generic timestamp (t_{event}) is the combination of the coarse and fine ones; i.e., $t_{\text{event}} = T_{\text{COARSE}} - T_{\text{FINE}}$.

that extends the FSR. As shown in Fig. 7, the "stop" of the TDL-TDC is connected to a clock that also drives the digital counter. In this way, the measurement of the instant of occurrence of an event ("start" of the TDL-TDC in Fig. 7) can be seen as the combination of a fine measurement (T_{FINE}), performed by TDL-TDC, which can be seen as the time interval between the instant itself and the clock, and a coarse one (T_{COARSE}), provided by the counter as the counter value itself. In this manner, the precision is due to the combination of the precision offered by the TDL-TDC and the clock jitter; in this sense, a stable (<100 ppm) and low-jitter (<90 fm rms) 2.4-ns external clock is used [28]. In this way, the nonidealities of the coarse contribution are negligible with respect to the fine ones.

In the CDL context, it is easy to understand how the TDC must feature at least four channels (each one based on the Nutt interpolation of a TDL-TDC and a coarse counter), called "STOP" (the uppercase is used to distinguish with the "stop" signal of the TDL-TDC), one for each end of the two meanders of the detector: to obtain spatial information, two CDLs are needed (X- and Y-directions), each of which with two terminations to be read out. Moreover, a fifth channel, identical to the four STOPs and called "START" (the uppercase is used to distinguish with the "start" signal of the TDL-TDL), is present: it is connected to the reference trigger of the experiment (see Fig. 8). In this manner, it possible to compute the arrival time of the STOPs referring to the START.

The TDC features a pipeline structure, which allows to achieve an extremely short dead time of 7 ns. This short dead time ensures that all the pulses from CDL can be captured without losses, improving the overall efficiency of the system for multiple consecutive events arriving on the same input.

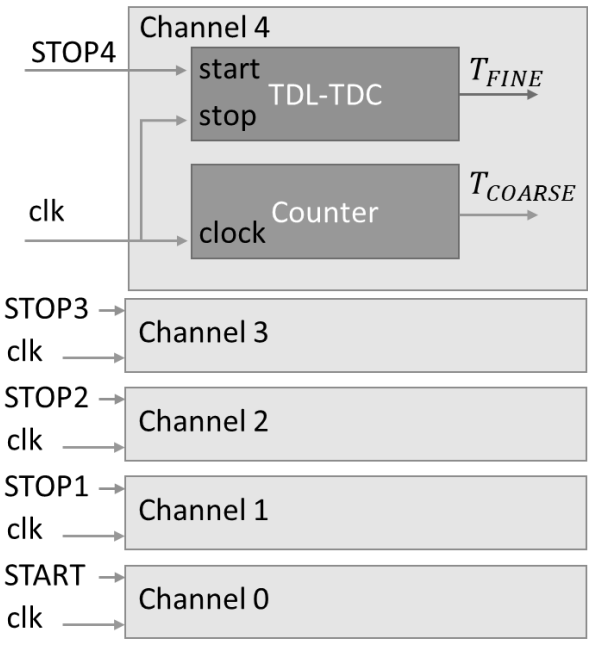


Fig. 8. Four STOPs and the START signals connected to the TDC channels. Detail of TDC internal logic, only for Channel 4.

TABLE II
PERFORMANCE OF THE PROPOSED FPGA-BASED TDC

Feature	Value
Number of Channels	4 + 1 Sync
Maximum Dead Time	7 ns
Maximum Channel Rate	10 Mcps per Channel
Channel Resolution (LSB)	2.17 ps
Channel Precision	< 12 ps r.m.s.
FSR	0.145 ms
INL	< 4 ps over a range of 500 ns

The TDC firmware is implemented on a Xilinx Artix[1]-7 XC7A200T-1FBG484 FPGA and is designed to provide high signal integrity, minimizing ground bounce, channel crosstalks, and clock jitters. In particular, thanks to an accurate design, the high performance achieved (imputable, in first approximation, to the TDL) in terms of precision (12 ps rms) and INL(4 ps over a dynamic range of 500 ns) are primarily reflected on the excellent quality of the image, which is reconstructed with a spatial resolution of 45 μm rms, and in the total absence of local distortions.

D. System Control and Data Processing

The system control and data processing tasks are accomplished by means of the FPGA-SCDP, an Intel 28-nm Cyclone-V FPGA. It receives the timestamps from the FPGA-TDC through an first in first out (FIFO)-based approach and immediately converts them into an extended format timestamp word with selectable bin width (typically around 2.17 ps or below), which delivers the absolute arrival time information of the hits detected on each channel with respect to the start of the acquisition or to a specific reference signal.

Through a software graphical user interface (GUI) (e.g., a LabVIEW application or a Python script) on the control PC, the system settings inside the FPGA-SCDP can be adjusted to best comply with the specific requirements of the detectors in use (2-D CDL, 1-D delay line, or multichannel anodes) and of the experimental setup (e.g., time-resolved operation mode, external triggering, external gating). In the most general case of time-resolved experiments using a CDL, careful tuning of the system settings allows to thoroughly filter and combine the incoming extended format timestamps, leading to the determination of the precise 2-D position and time of the detected events. The outcome of the processing is a flow of (X, Y, t) data which are transferred to the PC, where the software can perform further processing aimed at displaying live time-resolved 2-D images or even more advanced analysis on incoming data.

IV. EXPERIMENTAL EVALUATION

The various components of the imager have been tested in several different operative conditions.

The CDL and the A/D front-end have been fully tested in previous publication [11], where it is demonstrated an achievable spatial resolution better than 100 μm if referred to the THR02-TDC. For this reason, before presenting the images acquired on the final experimental setup (i.e., the detector placed in an experimental chamber in high vacuum) and showing the comparative tests between the THR02-TDC system and the ELETTRA-POLIMI system (see Section IV-B), in Section IV-A we will report the results regarding the bench characterization of FPGA-based TDC.

A. FPGA-Based TDC Characterization

First, an accurate delay scan with subnanosecond (10 ps) delay steps on a short time range, around 10 ns, using a mechanical delay unit, allowed to have an evaluation of the achievable channel-to-channel FWHM precision with the standalone FPGA-TDC: this can be as good as 35 ps, i.e., 14.9 ps rms (see Figs. 9 and 10).

It should be noted, referring to Fig. 10, that the FWHM precision resulting from the graph was computed by performing the analysis on the difference between two channels, e.g., X1 and X2 of Fig. 9; which means that each single channel has a contribution of $35/(2)^{1/2}$ ps, that is, 24.7 ps of FWHM (10.5 ps rms) in accordance with the TDC precision reported in Table II.

Bench tests much closer to the real high vacuum situation were performed using the entire acquisition chain, with the sole exception of the MCPs. The setup used is shown in Fig. 11. A signal suitably shaped so as to have the same characteristics as the one measured at the output of the MCPs is injected into different regions of the CDLs; then the signal propagates as previously described, i.e., it passes through the amplification stages, through the CFDs, and then, transformed into a digital pulse, and reaches the TDCs. Fig. 12, which reports the measurement of the temporal precision, is particularly meaningful, as it considers all the possible

[1]Registered trademark.

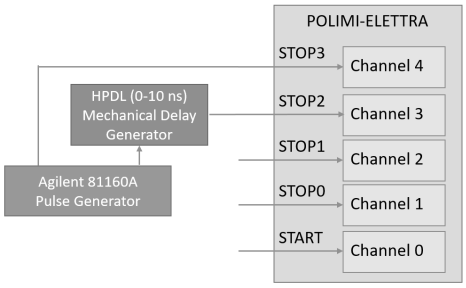


Fig. 9. Setup for the fine range scan.

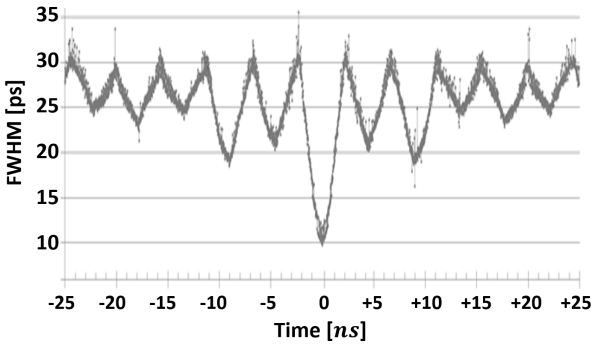


Fig. 10. FWHM precision for the POLIMI-ELETTRA system (combination of five fine scans, spanning 10 ns each).

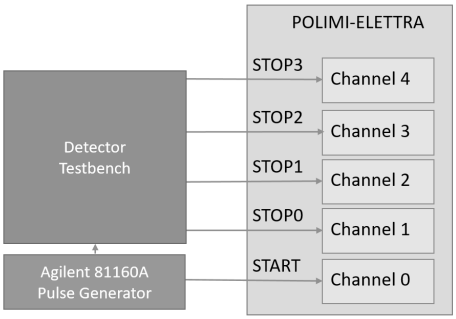


Fig. 11. Setup for the wide range scan.

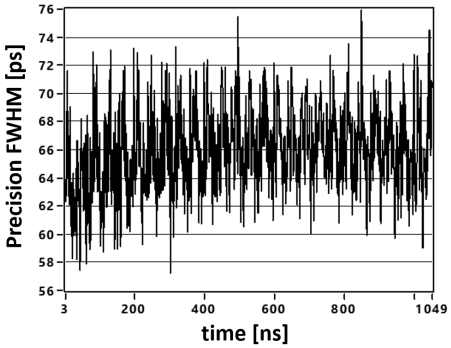
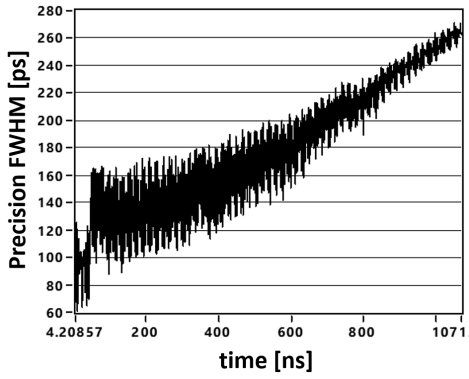


Fig. 12. FWHM precision for the double-FPGA system on the 1 μs range.

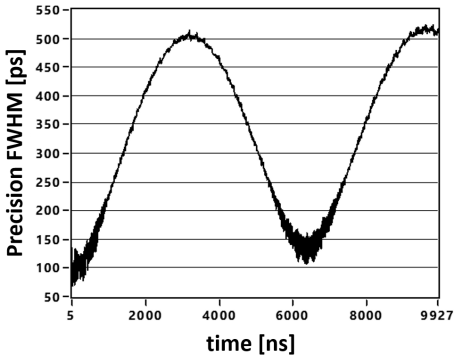
contributions to the jitter introduced by the various stages, and therefore, it is an indicator of the performances of the whole detector system. It can be seen that the precision of the temporal measurement between two events has an rms value equal to 32.3 ps and peak-to-peak between 60 and 70 ps and these values remain constant over time (the measurement refers to 1 μs of maximum temporal distance). These values are far better than what can be obtained with the state-of-the-art pixel detectors traditionally used for these applications, consisting of phosphor screen followed by CCD. In fact, the timing resolution of such devices is usually rather low (hundreds of microseconds or, limited to a stroboscopic mode of operation, few ns), and even in the configurations which are more specifically designed to reach high time resolutions [29] at the moment it is possible to achieve, in the best case, 750 ps [30], [31], [32]. It should also be emphasized that a time precision below 50 ps is notable even whenever compared with other works describing detectors in the state-of-the-art explicitly made to have excellent time resolutions, such as cross delay anode detectors [11], [33], [34], cross strip line detectors [35], [36], or detectors based on wedge strip zig (WSZ) charge division readout [37], [38]. In fact, when the precisions of other systems described in the literature reach 10 ps, electronics are based on a TAC approach rather than using TDCs. When using TAC, however, the excellent precision trades off with the ability to reach high count rates and makes it impossible to receive multiple pulses on the same channel, unless they are separated at least a few hundred nanoseconds. This second aspect, in particular, is unacceptable for many time-resolved measurements (e.g., in the case of time-of-flight measurements) for which the probability of receiving, within few nanoseconds, successive pulses on the same channel is very high. In the case of the system proposed in this work, it is possible to go down to a pulse-pair resolution of 7 ns, a value substantially limited by the propagation delays inside the FPGA. If we limit the comparison to systems based on TDC ASICs, the bench setup is ideal to compare the contribution of the TDC section in the two cases, given that the "CDL-amplifiers-CFDs" sections are the same in both the systems. In the case of THR02-TDC (based on the commercial ASIC-TDC-GPX), very dramatic relationship between FWHM and time is observed for intervals bigger than 100 ns, as shown in Fig. 13(a) and (b), and for the same time interval of 1 μm, an accuracy almost 10 times worse than that measured with the FPGA-based system is achieved; this behavior strongly limits the usability of THR02-TDC in experiments where it is necessary to measure time intervals longer than a few hundred ns with great precision. Finally, the setup allows to estimate the spatial resolution that can be reached by the detector, since the propagation delays along the delay lines are known. Considering that in a 50 $\times$ 50 mm CDL detector the average time taken by the electromagnetic pulse to go from one end to the other is about 20 ns, this means that the pulse moves along the two directions at a speed of about 2.5 μm/ps. Consequently, bearing in mind that a shift in one direction will delay the arrival of the impulse on one end and anticipate it on the other, a time precision of 15 ps rms translates into a spatial precision of 19 μm rms, or 45 μm FWHM.

B. Imaging Capability

New imagers normally get validated by a comparative approach with preexisting solutions. The POLIMI-ELETTRA system imager has been assessed several times with the



(a)



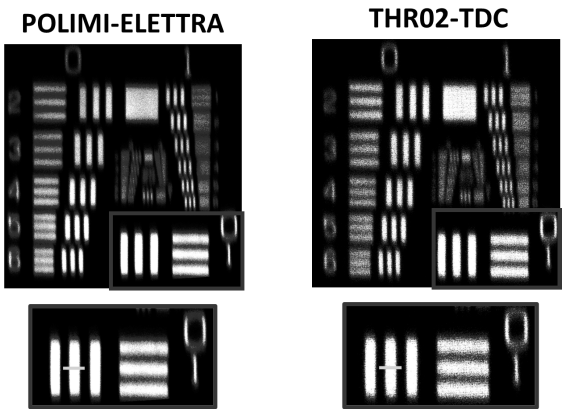
(b)

Fig. 13. FWHM precision of TDC-GPX (a) Short range; i.e., 1 μs range. (b) Long range; i.e., 10 μs range.

former THR02-TDC imaging system. In this measurement setup, POLIMI-ELETTRA and THR02-TDC are connected to a complete set of MCP, CDL, and A/D front-end illuminated by a proper light source. A standard USAF mask is interposed between the ultra violet (UV) light source and the MCP to properly investigate and evaluate the performance in terms of resolution and distortions (see Fig. 14), in particular to have evidence of possible undesirable crosstalk effects between the TDC channels.

Fig. 14 shows the images acquired with the proposed system and with the commercial TDC THR02 in the complete configuration traditionally used in the experimental chambers: although the mask is placed for safety reasons (the MCPs are floating at high voltage) a few mm from the MCPs, and consequently the resolution is partially degraded, it is still possible to observe that the images do not present distortions and that the spatial resolution of the image acquired with the FPGA-based system is remarkably higher. This can be better appreciated using the usual step-edge test technique (also known as knife-edge test [39]), as shown in Fig. 15; where a line profile of a section of the mask image (see Fig. 14) was made and the space required to go from 10% to 90% of the maximum value was evaluated [40]. In this, an image pixel of 27.8 μm and a profile of 70 μm are achieved with the POLIMI-ELETTRA system while of an image pixel of 35.6 μm and a profile of 107 μm are achieved with THR02-TDC.

Moreover, we would like to underline that the spatial resolution of the "system evaluated with bench measurement"



(a) (b)

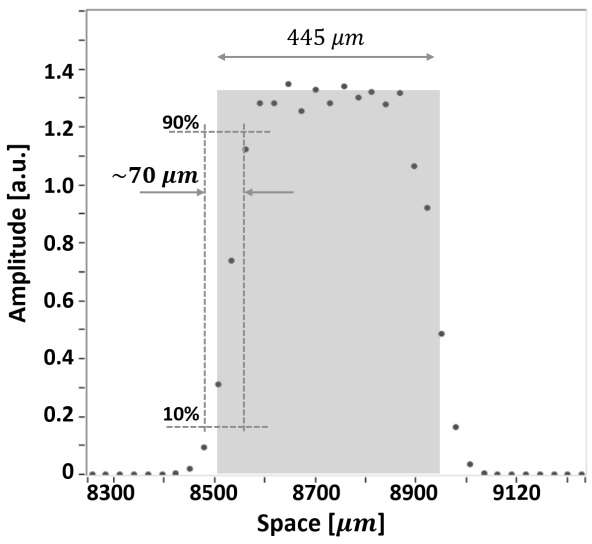
Fig. 14. POLIMI-ELETTRA system imager versus THR02-TDC imaging system where in green is highlighted the line profile reported in Fig. 15. (a) Image acquired with the USAF mask using the POLIMI-ELETTRA system. (b) Image acquired with the USAF mask using the THR02-TDC system.

(19 μm rms, or 45 μm FWHM) in Section IV-A is the time precision (15 ps rms) translates in space through the scale factor (2.5 μm/ps). This figure of merit is reported only to define an upper limit to the maximum achievable resolution with respect the real case of Figs. 14 and 15 where MCPs in vacuum are used.

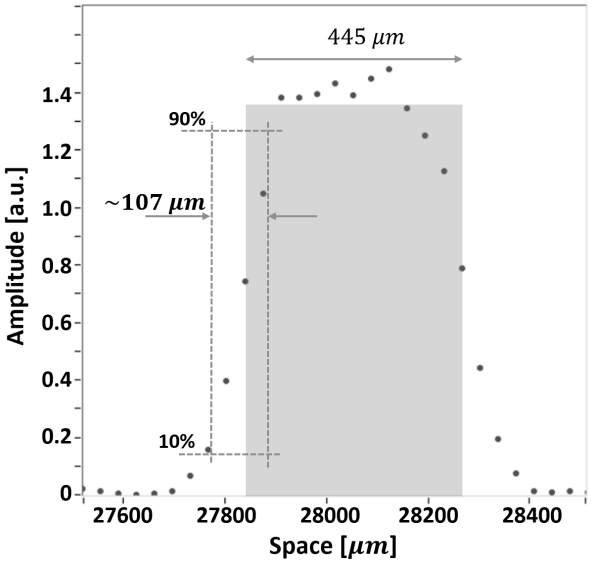
V. Future Developments

Some major improvements are in the process of being implemented along with the design of new FPGA-TDC and FPGA-SCDP PCBs and the migration, on the FPGA-SCDP side, from the Intel 28-nm Cyclone V to the Intel 20-nm Cyclone 10 FPGA to increase the computing power. Moreover, the signal integrity may be further improved using fully differential signaling for dedicated clocks and crucial timing endpoints: this is expected to bring a drastic reduction in crosstalk effects and improvements in the precision and accuracy of the measurements. Another significant upgrade will be the replacement of the FIFO-based approach, initially used for the communication between the two FPGAs in the system, with the use of fast serial communication using transceivers; similarly, the data acquisition output may be accomplished using gigabit transceivers, further improving the data transfer rate.

The data processing part is now mainly intended for the manipulation of the data coming from a single 2-D or 1-D detector, as for the typical case of a CDL detector used in electron analyzers in place of a CCD, for spectroscopy purposes which could benefit some time-resolved features. In the future, data processing might be subject to further developments. In fact, the availability of a higher (though obviously not unlimited) number of channels in FPGA-TDC paves the way for more complex experimental scenarios in which more than a single position detector is used in parallel. However, besides the attractive advantage of being able to preview the live images coming from the position detectors in the system, the general approach is that of providing to the end user a way to access both the processed data and the



(a)



(b)

Fig. 15. Line profile performed on a line of the USAF resolution test mask image; the blue rectangle represents the ideal profile (green line in Fig. 14), and the dotted line the measured one (a) POLIMI-ELETTRA system with a step of 27.8 μm (image pixel) and a profile of 70 μm (precision). (b) THR02-TDC system with a step of 35.6 μm (image pixel) and a profile of 107 μm (precision).

unprocessed "raw" ones. This may be made available, as a benefit of the improvements in the data transfer rate, with the general upgrade of the double-FPGA system.

In the preliminary upgrade of the system, the number of TDC channels has already scaled up to 8 without the evidence of any detrimental effects on various indicators of the performance of the system. The further ongoing evolution of the system will be subject of a forthcoming publication.

VI. Conclusion

An efficient imager based on time-to-space conversion has been proposed.

The front-end of the system exploits a CDL detector and is combined with a fully digital stage constituted of two separate FPGAs, the first (FPGA-TDC) essentially dedicated to the time-to-digital conversion and the second (FPGA-SCDP) to the processing of the signals coming from the FPGA-TDC and the subsequent live reconstruction of images.

The proposed solution allows to achieve a spatial resolution of 45 μm FWHM and a time precision of 15 ps rms at a maximum channel rate of 10 Mcps with a minimum dead time (event-to-event minimum time) of 7 ns. The imager is extremely versatile and adaptable to a wide spectrum of application scenarios, and this solution is the first step toward a valid alternative to the current (x, y, t) TDC-based detectors. Although some aspects can be improved, the performance of the developed device described in this work is comparable and, in some respects, even better than what is currently available. For this reason, the use of the system in experiments with synchrotron light has been planned: in this way, we will have the opportunity to test the high degree of configurability of the system and to bring out criticalities that are not detectable with measurements in the laboratory.

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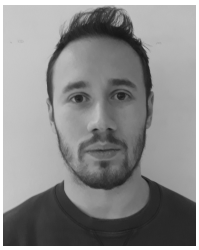
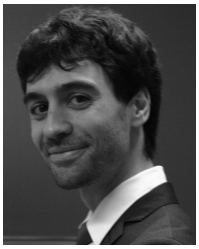


Marco Cautero received the bachelor's and master's degrees in electronical engineering from the University of Trieste, Trieste, Italy, in 2020, where he is currently pursuing the Ph.D. degree in collaboration with the Instrumentation and Detectors Laboratory, Elettra Sincrotrone Research Center.

His current studies are focused on the development of field programmable gate array (FPGA)-based electronic instrumentation for applied physics and GaAs separate-absorption-multiplication avalanche photodiode (SAM-APD) and ultrafast photoconductive switches.



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His research topic is focused on advanced programmable logic (PL) and software architectures for data processing and transfer in field programmable gate arrays (FPGA) implemented scientific equipment, currently used, and developed together with the time-to-digital converter (TDC) and digital-to-time converter (DTC) developed with the Digital Electronics Laboratory.

Gabriele Brajnik received the M.S. degree in electronic engineering from the University of Udine, Udine, Italy, in 2012, and the Ph.D. degree from the University of Trieste, Trieste, Italy, in 2017.

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Since then, he has been working with the Instrumentation and Detectors Laboratory of the ELETTRA Synchrotron Lightsource, Trieste. Being involved in the development of the hardware and software for field programmable gate array (FPGA)-based acquisition systems for scientific instrumentation, he has gained a year-long experience in Verilog high description language (HDL) and LabVIEW programming.

Rudi Sergo has been working with the Elettra Sincrotrone Trieste Research Center, Trieste, Italy, as an Electronics and Mechanics CAD Expert Designer. Since 2007, he has held courses in "high speed PCB design techniques" at the engineering faculty of the University of Trieste, Trieste. He is the coauthor of about 50 scientific publications and holds a patent. His main research lines concern the design and development of constant fraction discriminators (CFDs), time-to-digital converter (TDC), and RF amplifiers.

Giuseppe Cautero received the M.S. degree in physics from the University of Trieste, Trieste, Italy, in 1990.

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