System Stability and Short Circuit Contribution as Discordant Targets in Cascade Connected DC Microgrids: a Design Procedure

Andrea Vicenzutti, Daniele Bosich, Andrea Alessia Tavagnutti, Giorgio Sulligoi
Dept. of Engineering and Architecture
University of Trieste
Trieste, Italy
avicenzutti@units.it, dbosich@units.it, andreaalessia.tavagnutti@phd.units.it, gsulligoi@units.it

***Abstract*—Advanced DC microgrids design requires considering interdependent aspects. In these flexible grids with large penetration of high-bandwidth controlled converters, both system stability and short circuit limitation are crucial aspects to be attained. The design of filtering stages directly affects both: on one side the stability is beneficially influenced by a large filter capacitor, while on the other the short circuit current increases with oversized capacitors. Thus, voltage stability and filter's short circuit contribution are discordant goals, which need to be carefully balanced by the designer. To solve this issue, a design procedure for sizing the LC filtering stage and the main bus voltage in a cascade-connected DC power system is proposed. The aim is to ensure meeting both voltage/current ripple requirements, as well as accomplishing system stability and limiting the energy supplied into a fault. Final tests on a Hardware-In-the-Loop system and electro-magnetic transients' simulations are used to verify the effectiveness of the filter's designing procedure.**

Keywords—DC microgrid, LC filter, stability, power quality, short circuit.

I. Introduction

In several power systems' applications (e.g., microgrids [1-2] and vehicular [3-6]), the DC technology is demonstrating its capability as an enabler for pursuing the sustainable energy goals [7]. While the extensive use of controlled power converters in modern DC systems ensures real-time power and voltage control, it also causes specific issues [8]. Indeed, when large is the number of filtered interfaces to the bus [9-10], the dynamics interaction between high-bandwidth controlled converters and their LC filtering stages may induce system instability [11-12]. To solve such an issue, a procedure for the stability-oriented filter design in a DC cascaded-system has been discussed in [13], aimed at guaranteeing both the power quality requirements compliance and the system stability. Such procedure reaches its goals by dropping the maximum allowable control bandwidth for the load side converter (thus limiting its performance). However, in a cascade connected system additional degrees of freedom may be available for the designer, possibly allowing to reach the same filtering goal with a different set of parameters. Among the available ones, the most significant degree of freedom is constituted by the bus voltage selection. The latter can be freely adjusted (up to a certain extent) in a cascaded-connected DC system, being all the connected sources and loads interfaced by controlled converters. Such choice increases the number of feasible solutions for the filtering stage definition, thus allowing to optimize it towards additional goals like the minimization of the energy supplied by the filter to a short-circuit on the DC bus [14].

Given these premises, in this paper a revision of the design methodology of [13] is proposed. The procedure here described takes the bus voltage as an additional variable, from which some of the parameters that were previously fixed by the designer are obtained. Moreover, a new design step is appended, to evaluate the energy stored in the filter (which is injected in the fault if a short circuit on the main bus happens), and provide its reduction below an acceptable level. By means of these new steps, the procedure becomes easier to apply in respect to the original one, and allows meeting an additional goal (i.e., the fault energy reduction). Although the topic of DC short-circuit has been largely investigated, also in recent years [15]-[17], this paper provides a different insight, focusing on the interactions between DC system stability and fault contribution.

The paper is organized as follows: Section II presents the case study for the design procedure application; in Section III the design procedure is described; the results of the design procedure are in Section IV, using both Typhoon HIL emulation and electro-magnetic transients' simulations to demonstrate its effectiveness; finally, Section V provides the paper conclusions.

II. Cascaded connected DC microgrid case study

The methodology in this work applies to power systems integrating a set of buck converters supplying a main DC bus, to which other buck converters take power to feed the loads. The case study power system is in Fig. 1, where two cascade connected buck converters are present. While the system here considered is simple, it is representative of more complex ones. Indeed, if multiple load and suppling converters are connected to the same bus, aggregation of the generating converters on one side and of load converters on the other can be made, making it possible to develop an equivalent model like the one in Fig.1. In the figure only the voltage control of the load converter is depicted, due to the possibility of ignoring the upstream converter's control systems for analyzing the main DC bus voltage stability [13]. However, the supplying converter is endowed with both current and voltage controls, and their effect becomes relevant in the short circuit simulations results shown in Section IV. One strong hypothesis that must be met for applying the proposed design procedure is that the load converter control bandwidth (ω_2) should be sufficiently smaller than its output filter resonance frequency (ω_{f2}). This allows using the third order model hypothesis for the stability analysis [13], i.e., making it possible to neglect the load converter filter.

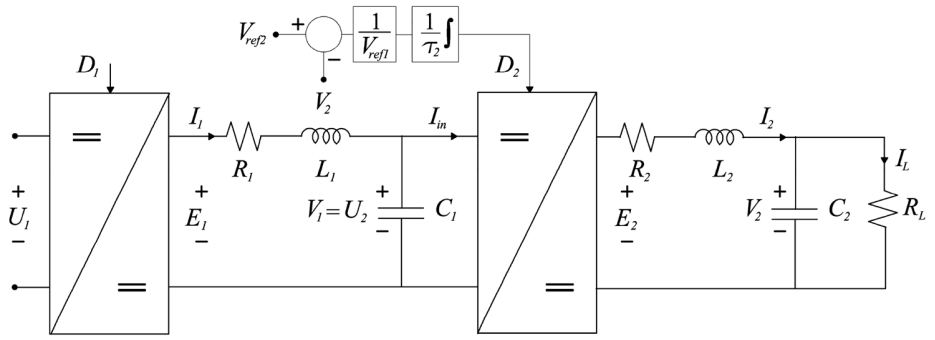

Fig. 1. Cascade-connected DC power system [13].

To provide an example of the results achievable with the proposed procedure and allow its demonstration, a case study system is here hypothesized, using data taken from [12] and [13]. The suppling converter switching frequency (f_{s1}) is set to 1500 Hz, it rated power (P_1) is 15.750 MW and its input voltage (U_1) is equal to 8910 V. Regarding the load converter, its output voltage (V_2) is 4800 V, the rated power (P_2) is 13 MW and the switching frequency is set to 3000 Hz. A minimum control bandwidth of 600 rad/s is set for the latter, to guarantee the correct control of the load. The load converter filter is defined following the load power quality requirements, but being the procedure applying the third order hypothesis it is ignored. Finally, the voltage and current ripple limits for the main DC bus are set to 3% and 15% respectively. It is relevant to notice that the proposed procedure is generally applicable to all the DC power systems having the structure above-depicted, and the input parameters can be freely chosen by the designer (e.g., following standards requirements, or contractual requirements).

III. Design Procedure

The design procedure is aimed at finding a suitable combination of the load converter 1 output filter parameters (Fig. 1) and the main DC bus voltage (V_1). The procedure here discussed requires defining only few parameters at the beginning of the design procedure, allowing to obtain the other ones as the output of the optimization process. The input parameters are strictly related to the requirements of the system in design: rated power of the supply converter (P_{n1}); rated power of the load converter (P_{n2}); load converter control bandwidth (ω_2); load converter output filter resonance frequency (ω_{f2}); input voltage of the supply converter (U_1) and its nominal value (U_{n1}); output voltage of the load converter (i.e., nominal voltage of the load, V_{n2}); main DC bus voltage ripple objective ($\Delta V_{\%1}$); main DC bus current ripple limit ($\Delta I_{\%1max}$); supply converter switching frequency (f_{s1}); maximum accepted short-circuit energy (W_{max}); expected losses of the conversion system (ΔP_{diss}) . In addition to these, the designer must make a starting guess in terms of maximum allowed load converter control bandwidth (ω_{2max}) and DC main bus voltage (V_1). Then, by means of the proposed procedure, the final bus voltage value and the L and C parameters of the converter 1 output filter can be obtained. The procedure also enables evaluating the effect that each variable has on the result, allowing to select the best compromise between stability and short circuit energy. Indeed, it is possible to iteratively apply the procedure over a range of variables (e.g., the possible DC main bus voltage), to trace the consequent output results' variation.

The step-by-step design procedure is described in Fig. 2 and exploits the equations depicted at the end of this Section (recalled in the figure using the same numbers used in the text). While the core of the procedure (i.e., the subsection allowing the determination of L_1 and C_1 values) is similar to the one in [13], in this revision the bus voltage is a variable that can be used to reduce the filter energy below a given limit. This is enabled by the controlled nature of the cascaded converters, which allows for some implementation flexibility. Indeed, voltage choices made to optimize filters can be compensated either by changing the control references (for small deviations), or by choosing another converter (for greater voltage deviations). The procedure starts by hypothesizing an initial value for the maximum load converter control bandwidth ω_{2max} and for the bus voltage V_1. For the former the initial guess may be to maximize the available bandwidth, thus setting an ω_{2max} as higher as possible (the design process decreases it if necessary). Conversely, the latter is limited on the upper side by the input voltage of converter 1, and on the lower side by the output voltage of converter 2 (being the converters using the buck architecture, they can only decrease the voltage between their input and output). Once identified a possible ω_{2max}, it is necessary to check if it is lower than ω_{f1} (resonance frequency of the supply converter output filter), to ensure voltage stability. Indeed, the load converter voltage control bandwidth must not intersect with the resonance frequency of the main DC bus, which is essentially given by the converter 1 output filter components. If such condition is not met, voltage V_1 is to be increased. Although the supply converter's filter resonance frequency ω_{f1} cannot be directly calculated (the filter parameters have still to be determined), it is possible to evaluate it from the main DC bus voltage ripple objective $\Delta V_{\%1}$ and the other available data. With the information on ω_{2max}, ω_{f1}, and R^* (1), the value of C_1 can be then calculated providing, along with other parameters, both the L_1 value and the estimated current ripple $\Delta I_{\%1}$. If the latter is lower than the maximum accepted value $\Delta I_{\%1max}$, then it is possible to move forward in the procedure. Otherwise, the ω_{2max} is to be lowered and the calculations must be repeated iteratively. The provisional capacitance value allows calculating the critical inductance value L_c, which separates Continuous Conduction Mode (CCM) from Discontinuous Conduction Mode (DCM) in a buck converter. If the provisional L_1 is greater than L_c, then the CCM

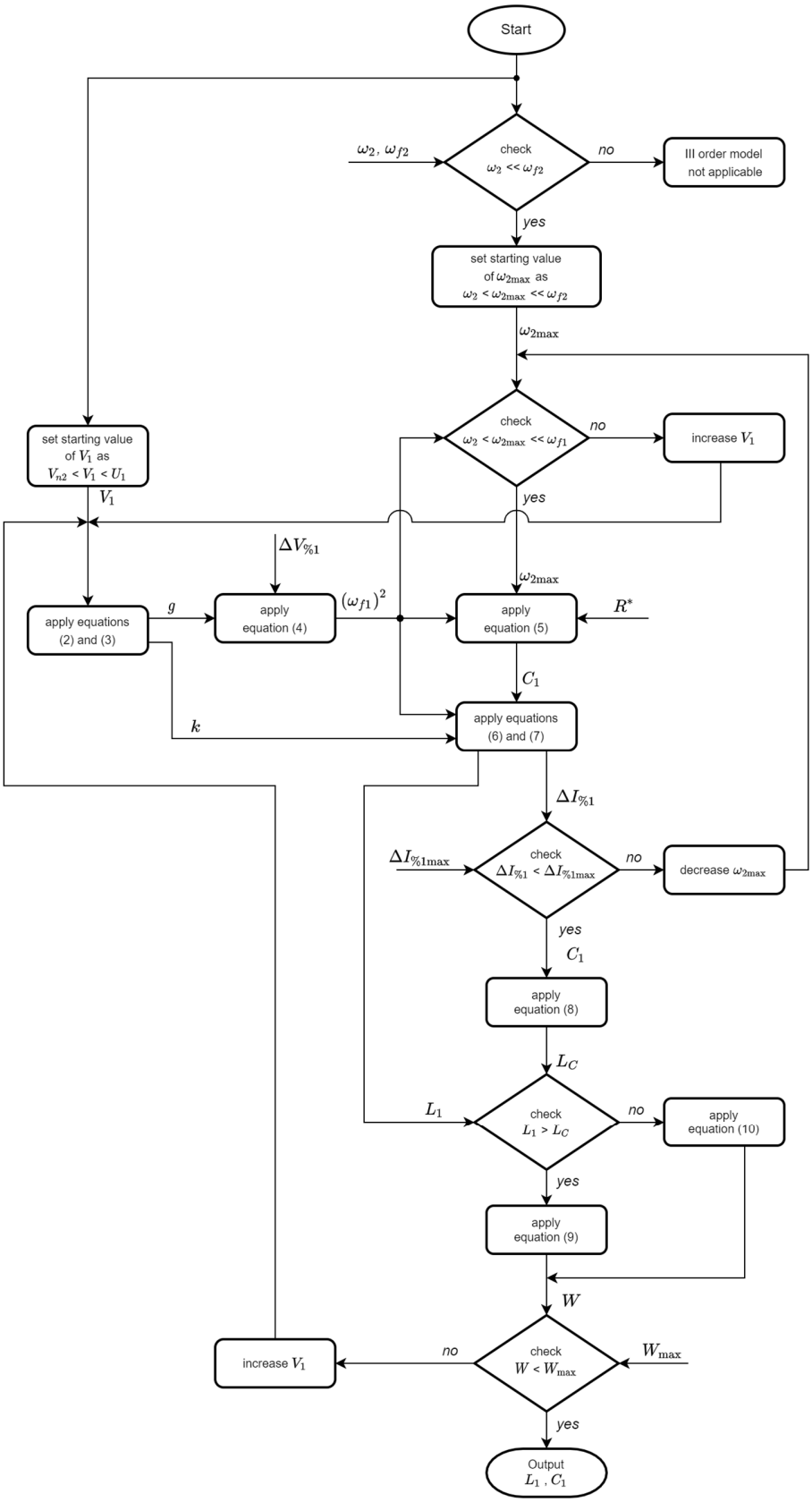

Fig. 2. Proposed design procedure.

equations for the energy stored in the LC filter can be used, else the DCM ones must be applied. The resulting energy stored in the filter W in Joule [14] (which is injected in the fault if a short circuit on the main bus happens) can finally be compared with the maximum accepted short-circuit energy W_{max}. The procedure is concluded if the calculated value is smaller than the required one, otherwise it is necessary to increase V_1 and iteratively repeat the procedure.

Being the DC bus voltage a design variable in the proposed procedure, the results may lead to the use of a non-standardized values. This is not an issue in some applications. An example can be made referring to the power conversion section of a drillship. In modern applications all the controlled loads (mostly pumps) are supplied through inverters, connected to a common DC busbar. The latter is obtained by means of a rectifying stage connected to the onboards AC busbars. In this configuration, the DC bus voltage is not accessible by any other load, and thus can be freely chosen by the designer of the conversion system following the power converters needs.

The equations used in the procedure, and recalled in Fig. 2, are depicted below. These are obtained as shown in [13] and [18]. The equations that are here used but are not present in the cited papers are obtained by simple elaborations of the reference ones. All the parameters and variables are defined in the above text, at the start of this section.

$$R^* = \frac{R_L}{D_{20}^2} \quad with \quad D_{20} = \frac{V_2}{V_{n1}} \; and \; R_L = \frac{V_{n2}^2}{P_{n2}} \tag{1}$$

$$g = \frac{1 - D_1}{8 f_{s1}^2} \quad with \quad D_1 = \frac{V_1}{U_{n1}} \tag{2}$$

$$k = \frac{(U_{n1} - V_1)(\frac{V_1}{U_{n1}})}{f_{s1} I_1} \quad with \quad I_1 = \frac{(1 - \Delta P_{diss}) P_{n1}}{V_1} \tag{3}$$

$$\omega_{f1}^2 = \frac{\Delta V_{\%1}}{g} \tag{4}$$

$$C_1 = \frac{\omega_{2max}}{R^* (\omega_{f1}^2 - \omega_{2max}^2)} \tag{5}$$

$$\Delta I_{\%1} = k \times \omega_{f1}^2 \times C_1 \tag{6}$$

$$L_1 = \frac{1}{\omega_{f1}^2 C_1} \tag{7}$$

$$L_c = \frac{R^* (U_{n1} - V_1)}{2 f_{s1} U_{n1}} \tag{8}$$

$$W \approx \frac{L_1}{2} \left[\frac{V_1}{R^*} + \frac{V_1 (1 - V_1 / U_{n1})}{2 L_1 f_{s1}} \right]^2 + \frac{C_1 V_1^2}{2} \quad for \; CCM \tag{9}$$

$$W = \frac{V_1^2 (U_{n1} - V_1)}{f_{s1} R^* U_{n1}} + \frac{C_1 V_1^2}{2} \quad for \; DCM \tag{10}$$

The procedure is set using as a primary objective the compliance with the power quality requirements. Indeed, the voltage ripple value $\Delta V_{\%1}$ is considered as an input data, and the procedure does not act on this value. Similarly, the current ripple $\Delta I_{\%1}$ is a working variable, but its maximum allowed value is a hard limit. To attain voltage stability on the main DC bus, the procedure acts on the load converter's maximum allowed control bandwidth ω_{2max}, while the filter energy limitation is attained by means of the main DC bus voltage V_1 variation. Due to the relations between these variables obtained during the simulations (refer to the following section), the effect of these two variables (ω_{2max} and V_1) can be represented by a monotone function. Thus, the procedure can be started using the greatest allowable ω_{2max}, decreasing it only if it is necessary. Conversely, the main DC bus load can be set at a low value, and increased to reduce the energy supplied by the filter to a fault.

In the next Section, the results of the application of the design procedure to the case study described in Section II are presented and discussed. Then, the power system is modeled in Typhoon HIL real time simulator to verify the power quality requirements, and an electro-magnetic transient (EMT) simulation is done to evaluate the system's behavior during a rail-to-rail short circuit fault on the bus.

IV. Results

Before presenting the simulation results, the outputs of the optimization procedure for the Section II case study are discussed. To provide an increased amount of information, the proposed procedure is applied iteratively to the case study, changing the V_1 voltage each time. This allows finding all the feasible filter designs in the allowed main DC bus voltage range, while the Fig. 2 procedure application provides a single feasible filter design given the input data set. The Fig. 3 depicts the obtained normalized filters and energy values over the bus voltage range, where the filter values (subscript *n* in the figure) calculated at 6000 V are used as reference point for comparing all the results. The filters values obtained for the 6000V base-case, as well as for other exemplifying bus voltage levels, are included in Table I. Figures 4 and 5 show the energy stored in the supply converter's LC output filter, calculated for each filter designed, and the maximum allowed load converter control bandwidth, respectively. The relation between the bus voltage and the other parameters is non-linear and some discontinuities are evident. No feasible filter design can be achieved at voltages lower than 5900 V and above 8900 V (a null value is set for all the parameters in such a case, for representation purposes only). The lower limit is given by the filter not meeting the condition regarding the minimum control bandwidth for the load converter (i.e., 600 rad/s) below such voltage, condition that requires a subsequent increase in the bus voltage to be solved as per Fig. 2 procedure. Conversely, the higher limit is given by the 8910 V voltage at the input of the supply converter. In all the figures a discontinuity is appreciable at approximately 7100 V, which is caused by converter 2 reaching its maximum allowed bandwidth (i.e., 900 rad/s) as visible in Fig. 5, which makes it impossible to increase ω_{2max} further.

To verify the validity of the methodology, the filter design obtained at different voltages have been tested by means of a model of the Fig. 1 system built in Typhoon HIL simulator. The results obtained for the 6000V reference design point are shown in Fig. 6, where the current and the voltage at the output of the supplying converter at steady state are depicted. From the results it is clear that the designed filter allows complying with the power quality requirements on the main DC bus (voltage ripple < 3 %, current ripple < 15%). Similar tests have been performed on other test cases and have given positive results, but are not included on this paper for the sake of simplicity.

The results coming from the electro-magnetic transient (EMT) simulation of the reference design point system after a rail-to-rail short circuit on the DC bus are depicted in Fig. 7. Using the same time scale for each of the Fig. 7 sections, the bus

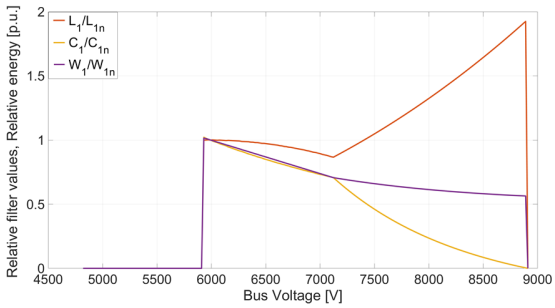

Fig. 3. Supply converter's output filter, filter parameters and stored energy, values in respect to the 6000 V reference design point (subscript *n*).

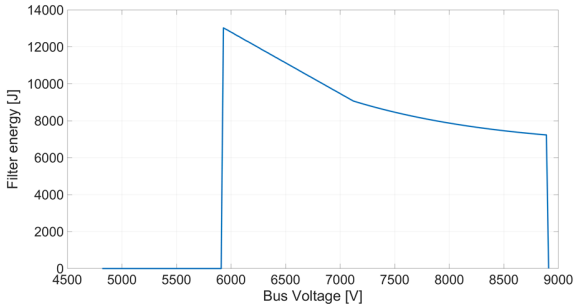

Fig. 4. Supply converter's output filter, stored energy.

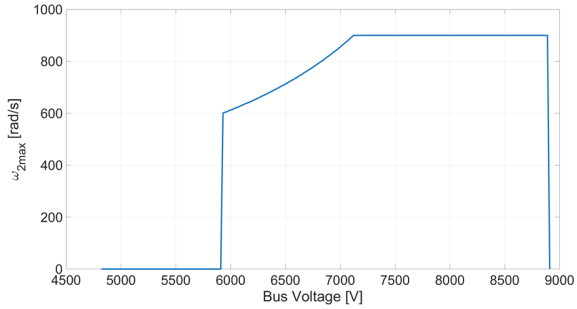

Fig. 5. Load converter maximum allowed bandwidth, limitation for mantaining main DC bus stability.

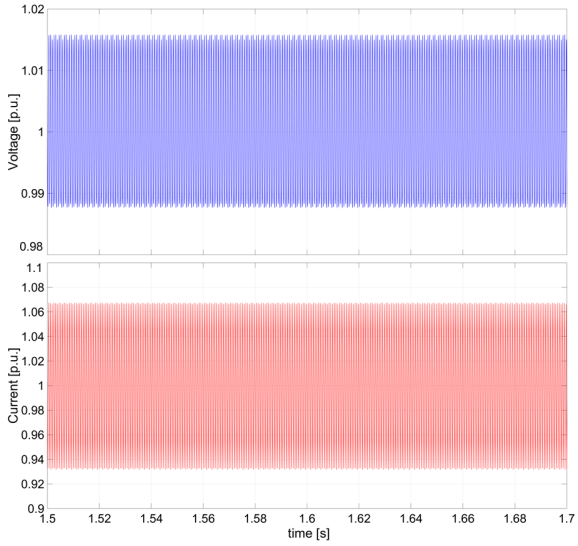

Fig. 6. Voltage and current ripple on the main DC bus at the 6000 V reference design point.

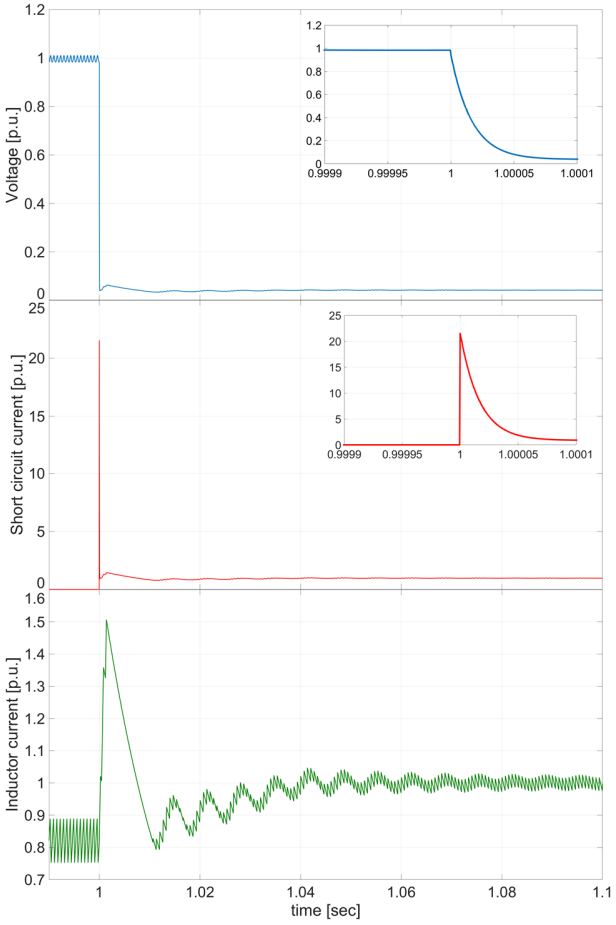

Fig. 7. Short circuit transients for a rail-to-rail fault on the main DC bus at the 6000 V reference design point: bus voltage, total fault current, and current in the inductor (L_I) of the supply converter's output filtering stage.

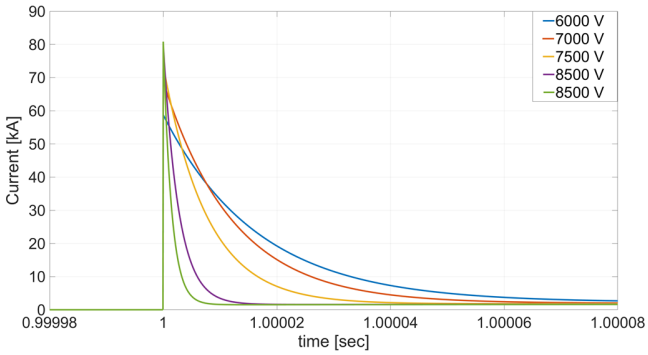

Fig. 8. Comparisons between the rail-to-rail short-circuit fault on the bus currents transients for different bus voltage levels.

TABLE I. JOULE INTEGRAL (I^2T) OF THE CURRENT FLOWING AFTER THE FAULT AND FILTERS' VALUES FOR DIFFERENT BUS VOLTAGE LEVELS.

Main DC bus voltage	***6000 V***	***7000 V***	***7500 V***	***8250 V***	***8500 V***
I^2t [A^2s] *10^8	6.3877	6.2566	4.5306	1.9365	1.1297
R [Ω]	0.126	0.172	0.194	0.240	0.254
L [mH]	35	31	37	52	57
C [mF]	0.173	0.127	0.081	0.026	0.015

voltage V_1, the fault current, and the current flowing through the filter inductor L_1 are depicted. For the first two variables a magnification of the transient is also given, to make it possible appreciating the current peak and the sudden decrease in the bus voltage. The current in the filter inductor is also the current at the supply converter's output, whose transient allows to highlight the converter's current control action. Indeed, after the first few moments of uncontrolled evolution, the output current is limited to its rated value. To provide a comparison among the different filter designs coming from the procedure, in Fig. 8 the fault current transient is depicted for five bus voltage levels. It is evident how the short circuit current peak gets higher as the voltage increases, due to the first capacitive discharge transient (i.e., $I_{cap} = C * dV/dt$). Nonetheless, the area under the curve becomes progressively smaller, and thus the energy discharged by the filter in the fault decreases. This can be appreciated also by means of the Table I results, where the Joule integral values of the rail-to-rail fault currents is depicted. The value is calculated for each case of Fig.8, considering a 4 seconds time frame after the fault event. Being the paper focused on the filtering stage design, no protection has been integrated. Thus, after the first fault transient where the capacitor energy is discharged, the fault current is limited only by the converter's current loop action. This allows to evaluate the effect of the filter on the fault energy, without having to compensate for different protection actions (e.g., different intervention times due to the effect of the filter inductance on the current derivative component). This is compliant to the results obtained from the procedure in terms of energy stored in the filter W (Figs. 3-4).

V. Conclusions

In the design process of DC power systems, the proper filter tuning is crucial to guarantee the power quality requirements, assure voltage stability, and mitigate the fault transients. Since these three objectives are conflicting, it is necessary to reach a compromise to obtain a filter that presents a satisfactory balance between them. In this paper a design procedure to attain such goal is proposed, applicable to cascade connected buck converters. The goal is to ensure the compliance with the power quality and stability requirements, while at the same time keeping the energy stored in the filtering stage lower than a certain limit (to contain the stress to the system components after a rail-to-rail fault event). The design process is clearly expressed in a flowchart, and the results are verified through circuital simulations. The stability of the power system as well as the adherence to the power quality requirements are indeed proven. Then is verified that the fault energy follows the expected trend. The methodology has proven to be effective for the design process of such DC power systems.

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