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Remote Laboratory for E-Learning of Systems on Chip and Their Applications to Nuclear and Scientific Instrumentation

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Abstract: Configuring and setting up a remote access laboratory for an advanced online school on fully programmable System-on-Chip (SoC) proved to be an outstanding challenge. The school, jointly organized by the International Centre for Theoretical Physics (ICTP) and the International Atomic Energy Agency (IAEA), focused on SoC and its applications to nuclear and scientific instrumentation and was mainly addressed to physicists, computer scientists and engineers from developing countries. The use of e-learning tools, which some of them adopted and others developed, allowed the school participants to directly access both integrated development environment software and programmable SoC platforms. This facilitated the follow-up of all proposed exercises and the final project. During the four weeks of the training activity, we faced and overcame different technology and communication challenges, whose solutions we describe in detail together with dedicated tools and design methodology. We finally present a summary of the gained experience and an assessment of the results we achieved, addressed to those who foresee to organize similar initiatives using e-learning for advanced training with remote access to SoC platforms.

Keywords: e-learning; SoC-FPGA; remote laboratory; nuclear instrumentation; scientific instrumentation; embedded processor

Citation: Crespo, M.L.; Foulon, F.; Cicuttin, A.; Bogovac, M.; Onime, C.; Sisterna, C.; Melo, R.; Florian Samayoa, W.; García Ordóñez, L.G.; Molina, R.; et al. Remote Laboratory for E-Learning of Systems on Chip and Their Applications to Nuclear and Scientific Instrumentation. *Electronics* **2021**, *10*, 2191. https://doi.org/10.3390/electronics10182191

Academic Editors: Juan M. Corchado, Stefanos Kollias and Javid Taheri

Received: 9 August 2021
Accepted: 3 September 2021
Published: 7 September 2021

1. Introduction

The Abdus Salam International Centre for Theoretical Physics (ICTP) [1] is a driving force behind global efforts to advance scientific expertise through advanced research and training of scientists from developing countries. Via its Multidisciplinary Laboratory (MLab), the ICTP conducts research on advanced scientific instrumentation, including the development of new instruments and associated methods, selecting the optimal hardware for implementing complex algorithms, and the use of cutting-edge technology to efficiently and effectively deal with big data or very high data rates.

ICTP, in partnership with the International Atomic Energy Agency (IAEA), [2] has organized for the last decade annual schools and workshops on Field Programmable Gate Array (FPGA) and fully programmable System-on-Chip (SoC) devices, as well as their applications for advanced scientific instrumentation [3–5]. These activities are normally face-to-face training events held at the ICTP premises and are open to scientists from different parts of the world. Participants are selected based on merit following an online application process. There are normally a number of grants available to support the

attendance of selected participants, with priority given to participants from countries that are members of the United Nations UNESCO [6] or IAEA, and there is no registration fee to attend the activities.

The limitations and concerns about COVID-19 stimulated the development of online schools and workshops at a global scale. It is crucial for these activities to have laboratories with e-learning tools so that participants can access and experiment on modern electronic platforms even from other countries. Providing such experimental setups and related tools, however, represents a real challenge. See for example [7], where remote laboratories and e-learning tools are discussed. In this paper, we describe the remote laboratory and the e-learning tools adopted and developed for the *International Online School on FPGA based SoC and its Applications to Nuclear and Related Instrumentation* that was jointly organized by ICTP and IAEA from 25 January to 19 February 2021 [8].

One of the aims of the ICTP-IAEA school is to provide key expertise knowledge to effectively take advantage of the fully programmable SoC technology, which combines multi-core processors with traditional FPGAs in a single chip. The inherent features of SoC-FPGA devices make them especially attractive for nuclear and scientific instruments, allowing multiple and parallel processing of signals from different sensor sources. Taking advantage of all the available resources of a SoC device requires the mastering of heterogeneous areas of competence rarely covered in university programs.

A central aspect is the hands-on experimental laboratory sessions, which are necessary to allow the participants to acquire critical know-how and the indispensable skills to exploit the cutting-edge technologies for scientific applications. Through direct experimentation with the assistance of highly qualified tutors, each participant grasps the real potential and limitations of the selected technology and associated design methodologies. The acquired knowledge will allow participants to autonomously increase their understanding of this topic and teach it to students in their home countries.

Despite the fact that ICTP and IAEA gained extensive experience in delivering international training courses over the years, they had to overcome the impossibility of in-person activities for the first time due to travel restrictions on this occasion. While theoretical lectures could be broadcast online, the experimental laboratory activities posed, instead, the challenge of allowing participants all over the world to have remote access to ad hoc hardware and experimental setups.

This paper is organized as follows. Section 2 presents the structure of the school, including its contents and the geographical distribution of participants and faculty members. Section 3.1 describes the Remote Laboratory, its hardware setups and software tools, and their use in the school. Section 3.2 presents the in-house development framework proposed as a base design for advanced SoC-FPGA project implementations. Section 3.3 provides a description of the school's laboratories and project activities. Section 4 summarizes the results from participants' survey and oral presentations. Finally, conclusions are discussed in Section 5.

Related Works

The literature review presents several efforts towards remote FPGA laboratories to enhance the learning process on these platforms. This is possible thanks to the growth of current technologies and online tools, together with the expansion of the Internet around the world.

Mohsen et al. [9] described an online laboratory based on Zynq and Virtex-7 kits, allowing multiple concurrent users with an assigned time slot and FPGA device and providing the student complete control over the FPGA. Video lectures and remote-lab based on FPGAs were presented in [10], connecting Argentina and Germany to overcome limitations such as different calendars, time zones, and cost of traveling. In this case, the FPGA board is connected to a server, where the student uploads the file to configure the board. Once the experiment is finished, the results are sent back to the student.

Another approach was presented in [11] to teach digital electronics using FPGAs (Nexys 3). A web application was implemented to avoid using webcams for feedback to users, creating a virtual representation of the board and its parts. A microcontroller was used to emulate peripherals that can be connected to the FPGA. Additionally, students must schedule a time slot to use the system. Authors in [12] described a remote laboratory with Nexys 2 boards for learning digital circuits design, using a remote viewer to access the PC and a webcam to observe the results in the FPGA, which is configured by loading the binary file generated by the student.

A framework for learning reconfigurable hardware was proposed by [13]. Each setup is comprised of a webcam, and a SoC-based board with external peripherals like remote switching controlling card and seven-segment displays. The students interact with the setup through a remote lab web interface. Lessons are supported by videos, lecture slides, and lab assignments. Authors in [14] developed an in-house FPGA cloud platform with multiple nodes based on Zynq UltraScale+ MPSoC.

Remote laboratories composed of reconfigurable FPGA devices were presented in [15], deployed and shared by institutions in Spain and Brazil to facilitate student access to this technology.

Although the idea of remote laboratories has been applied in different ways over the years, the previous works testify the academic interest in the implementation of remote learning for reconfigurable FPGA devices. In this paper, we consider a different scenario where the remote laboratory was applied in an international school, in which a wide spectrum of knowledge is taught in the framework of scientific instrumentation based on SoC. Under the hereinafter described conditions, the remote mode must resemble the experience the user would have when attending this type of hands-on-schools in-person.

2. International School

The school required potential candidates to apply online. The application was open to physicists, engineers, and computer scientists from all over the world. The selection of participants was made by the organizers of the school considering academic merits, motivation, reason for participation, gender equality, and geographic distribution; giving higher priority to candidates from developing countries. In total, more than 200 applications from 48 different countries were received. From them, 28 participants from 22 countries were selected.

Due to the variety and complexity of the school program, the faculty was a combination of international lecturers and laboratory tutors from different universities, scientists from various research centers, and professionals from hi-tech companies. A total of 23 faculty members allowed offering the participants solid academic resources and practical industry experience.

Participants and faculty members represented 26 different countries as shown in Figure 1. The complete list of names, institutions, and corresponding countries can be found on the ICTP school's website [8].

The school had a duration of four weeks. The daily timetable was set according to the Central European Time (CET) zone and split into two sessions, two hours in the morning, from 11:00 to 13:00, followed by three hours in the afternoon, from 14:00 to 17:00. The schedule was planned to allow participants from different time zones to follow both the lectures and laboratory activities. The morning sessions were mainly dedicated to theoretical lectures and demonstrations. The afternoon sessions were dedicated to tutorials, hands-on exercises, and experiments. The *Zoom* cloud-meeting software [16] was the communication medium utilized in both sessions. On the other hand, specific software applications were used for accessing the Remote Laboratory at any time, which will be described in the following section.

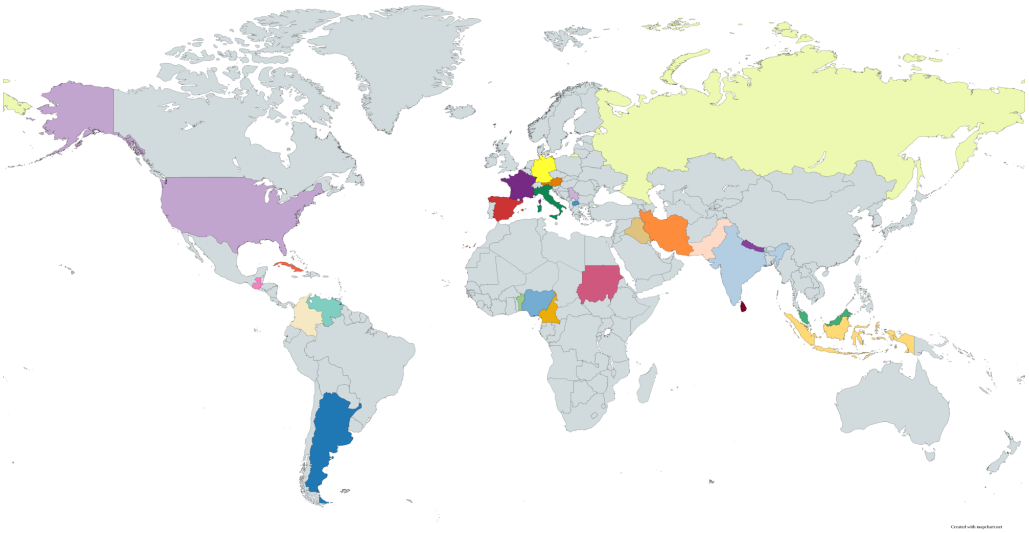

Figure 1. Geographical distribution of school's participants and faculty members. Represented countries are shown in color.

School Program

To provide participants with a common baseline of knowledge to carry out experimental laboratory activities, the school program included lectures on digital arithmetic circuit design, FPGA technology, SoC architecture and design methodology, hardware description languages (HDL), such as VHDL and HLS, embedded C programming, real-time operating system (FreeRTOS [17]), and demonstrations of the use of FPGA tools for machine learning acceleration (hls4ml [18]) and arithmetic core generations (FloPoCo [19]). Regarding nuclear and scientific instrumentation, a great level of technical implementation details was included in the lectures on front-end electronics and data acquisition systems for particle and radiation detectors. A detailed program of the school can be found on this ICTP website [20], along with the presentations of the lecturers in PDF format and video recordings of selected lectures.

The laboratory activities began at a basic level and progressed to reach complex designs. In the course of the first two weeks, the participants had the opportunity to get acquainted with the software design tools and state-of-the-art hardware platforms via the help of tutorials and specific hands-on activities. The exercises performed in these activities were developed by the MLab-ICTP. During the scheduled hands-on laboratory sessions, the participants were divided into six groups of about five people, each with a dedicated tutor. The tutor supervised and assisted the members of the corresponding group with the proposed experimental activities. Each group was assigned to a specific *Zoom Breakout Room* for these sessions.

Over the course of the school's last two weeks, the activities concentrated on the development of real application projects related to nuclear and scientific instrumentation. Two advanced projects were proposed to the participants: (1) Digital Pulse Processor for X-ray and Nuclear Spectroscopy, and (2) Data Acquisition System for Radiotracer Techniques in Industrial Applications and Environmental Monitoring. These projects are scientific instruments designed and implemented by the MLab-ICTP and the Nuclear Science and Instrumentation Laboratory (NSIL) [21] of IAEA, respectively. During the last two weeks, each group worked on one of the proposed final projects. The participants were encouraged to collaborate within their groups to accomplish the assigned project by contributing with their individual skills and the knowledge acquired during the school program.

As a final activity, the participants were invited to deliver a presentation on their experience regarding the implementation of the final project. These oral presentations, via *Zoom*, were scored by the participants and instructors and the three best-graded presentations received an award of Euro 200 each. During the closing ceremony of the school,

three types of certificates were issued for the participants: an attendance certificate, an oral presentation certificate, and an award certificate.

3. Materials and Methods

3.1. Remote Laboratory

An existing computer laboratory with 30 desktop computers was temporarily transformed as a remote laboratory for the duration of the school. The process involved the installation of a suitable version of Ubuntu Linux. Subsequent changes were made to the Network Firewalls to isolate the laboratory subnet from the rest of the network, allowing only the Dynamic Host Configuration Protocol (DHCP) and Domain Name System (DNS) traffic. Finally, additional firewall rules were also used to allow incoming Secure Shell (SSH) and Virtual Network Computing (VNC) connections from the Internet. Physically, each computer was connected to the network using a gigabit Ethernet connection, while the SoC hardware boards were all connected to the same subnet using a dedicated Fast-Ethernet switch. Thanks to the VNC and SSH connections, participants were granted access to a dedicated desktop computer with its installed software tools and the associated state-of-the-art SoC hardware platform.

Each desktop computer was connected, at minimum, to a ZedBoard [22] development board via USB. This hardware platform is based on a Xilinx Zynq-7000 SoC device [23] that integrates the hardware configurability of an FPGA with the software programmability of a dual-core ARM-based microprocessor in a single chip. The Xilinx Vivado Design Suite [24] was the Integrated Design Environment (IDE) used for project design (HDL and 'C') and implementation on the ZedBoard.

Using the described setup, the remote laboratory (computer and SoC-FPGA hardware boards) was available to all participants 24 h a day for the 4 weeks of the school program. In addition to being present during the scheduled assisted hands-on sessions, the participants could access the remote laboratory at any other time, although without direct assistance.

Laboratory materials were shared with all participants in a common repository based on *Git* [25]. The practical exercises and project assignments were associated with detailed tutorial guides to facilitate the autonomous work of the participants. A communication software application (*Slack* [26]) was also used as a forum for consultations and discussions among participants and instructors.

An overview of the Remote Laboratory architecture is shown in Figure 2. An extensive description of the hardware resources, ad hoc experimental setups, web services, and software applications used in the laboratory is depicted in the following subsections.

3.1.1. Hardware and Experimental Setup

Each remote laboratory workstation consisted of a desktop computer connected to the Internet, a ZedBoard connected to the computer via two USB ports (one for programming and the other for communication), and a USB webcam attached to the computer and pointing to the ZedBoard as a mode of providing real-time visual feedback to the participants on the various display elements available. Additional USB ports of the computer were used to connect other instruments utilized in specific hands-on sessions.

The ZedBoard is a development hardware platform for the Zynq-7000 ARM-FPGA all programmable SoC. Among the main characteristics of the ZedBoard that can be mentioned are an XC7Z020 FPGA IC, 512 MB DDR3 memory, a Gigabit Ethernet controller, JTAG programmer, an SD memory card interface, and several expansion connectors, Pmods [27] and FMC [28], bringing out programmable I/O pins from both the microprocessor and the FPGA. These features and the inclusion of on-board user's LEDs, switches, push-buttons, and various peripheral interfaces, made the ZedBoard ideal for developing processes as well as for educational purposes.

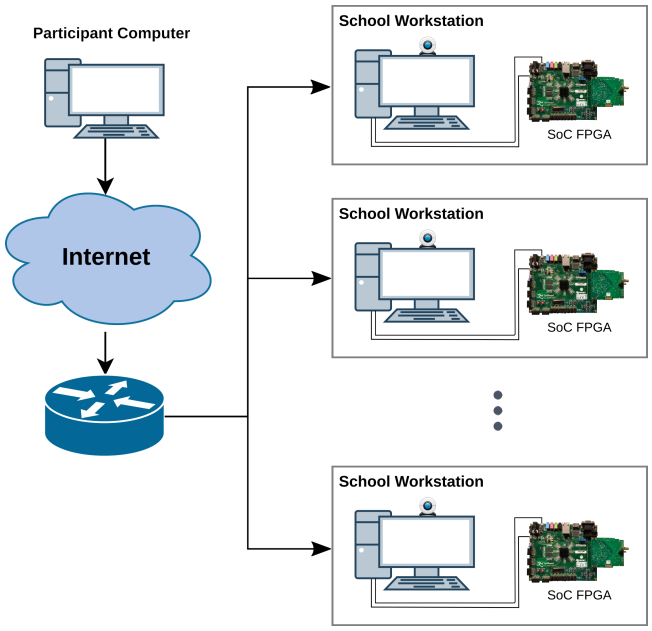

Figure 2. Overview of the remote laboratory architecture.

All the hands-on activities during the first two weeks of the school were done using just the ZedBoard. For some output data display and input data settings, a Digilent Analog Discovery 2 (Dig-AD2) instrument [29] was used. This is a multi-function instrument to measure, visualize, generate, record, and control mixed signals and it completely fits the needs for testing and measuring the ZedBoard I/O data.

As it was previously mentioned, the last two weeks of the school were dedicated to real application projects. To be able to carry out the two proposed projects, there were two different experimental hardware setups, one for the ICTP proposed project and the other for the IAEA proposed project, as described below:

- The ICTP hardware setup was based on a digital pulse processing system for X-Ray and nuclear spectroscopy, which was developed at MLab-ICTP. The system featured: a ZedBoard carrier card, an in-house high-speed data acquisition (DAQ) mezzanine card, a photo-multiplier tube (PMT) [30] with a scintillator crystal, a high voltage (HV) power supply, and a Dig-AD2 multi-function instrument. This setup is depicted in Figure 3.
  The DAQ card was designed at MLab-ICTP based on a commercial analog-to-digital converter that digitizes signals to 8 bits resolution at sampling rates up to 500 MHz (ADC500 [31]). It was connected to the SoC-FPGA carrier through an ANSI/VITA 57.1 FMC connector. The DAQ card [32] requires an external power supply provided by the Dig-AD2 instrument, which also generated signal stimuli for testing and calibration. The PMT was polarized using an Iseg BP40105n12 DC-HVDC converter [33] with programmable operation voltage. The output signal of the PMT was connected through a coaxial cable to the ADC500 input.
  For the evaluation of the final project, the participants tested their designs using synthetic pulses generated by the Dig-AD2 instrument and the PMT detector was connected to their remote hardware setup on request.
- The IAEA hardware setup was based on a radiation detection system for radiotracer applications in industry, which was developed at IAEA. The system consisted of multiple scintillator probes attached to a multi-port Power over Ethernet (PoE) switch. A single probe was used and attached to a single-port PoE switch to implement several identical training setups. Each probe consisted of a scintillator coupled to a PMT, a HV power supply board with a simple analog front-end (AFE) for converting anode pulse into voltage, and a digital pulse processing (DPP) board for data conversion and processing. The DPP board features a single-ended to differential amplifier, a 100 MHz

ADC, an Artix-7 FPGA module (CMOD-A7 from Digilent [34]), a Wiznet W7500P processor [35] for Internet connectivity, and a PoE module. The DPP board can accept analog signals from the AFE or a detector simulator. The FPGA can communicate with the computer using USB to UART bridge, or via Ethernet through the processor.

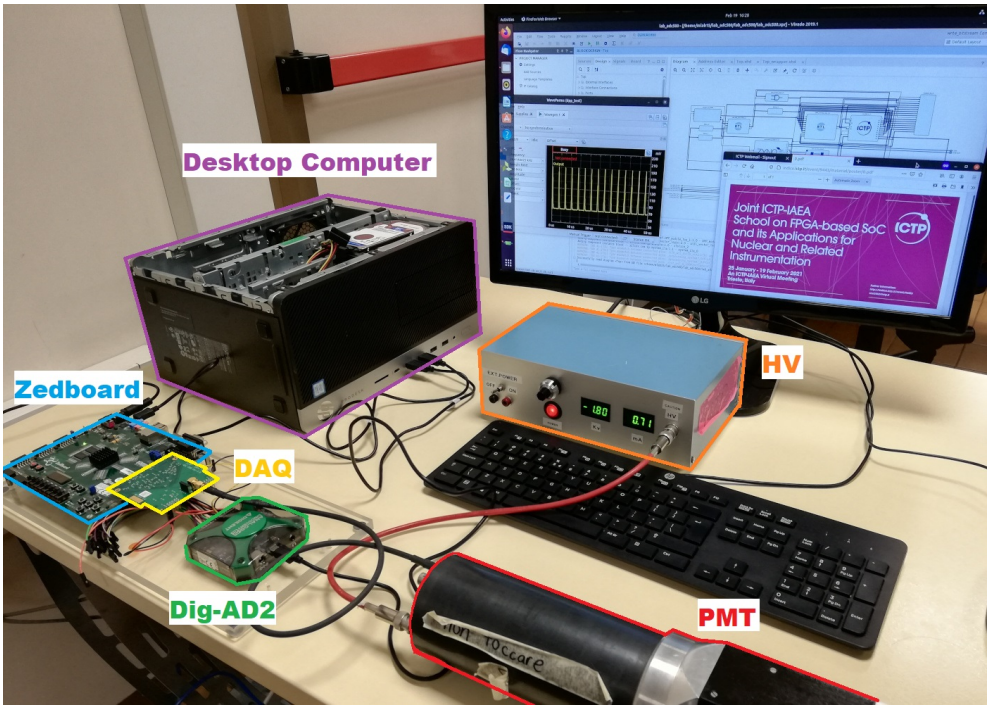

Figure 3. Experimental hardware setup for the remote laboratory.

3.1.2. Software Applications and Tools

The laboratory workstations were provided with all the software tools and applications needed for programming, connecting, and interfacing with the external hardware used in the experimental activities, as shown in Figure 4. Each workstation had an Ubuntu 20.04 [36] base installation with all the libraries and external drivers needed to work with the ZedBoard, the Dig-AD2 multi-function instrument, and the webcam.

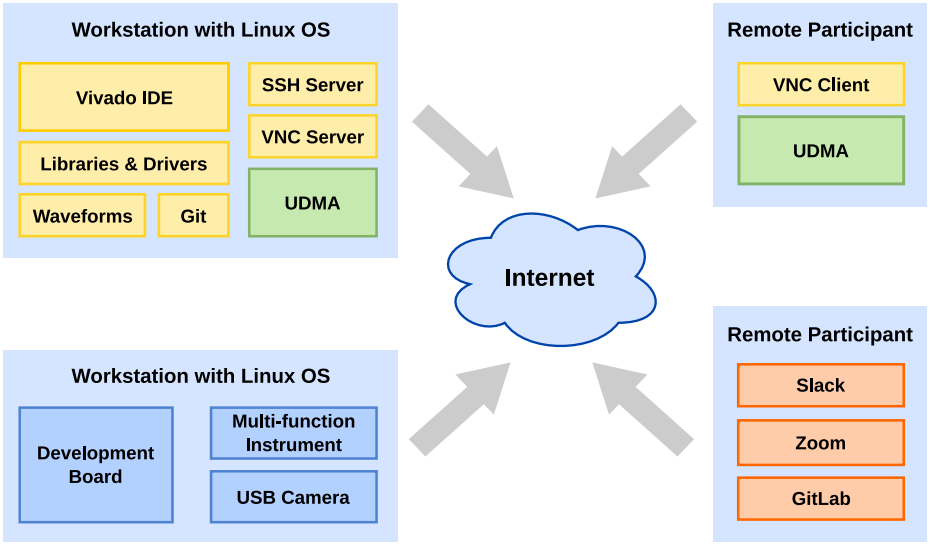

Figure 4. Software applications and tools for the remote laboratory.

Based on previous experiences, the Vivado Design Suite HLx Edition, version 2019.1, was selected as the main IDE tool to create the design, configure, and interface with the ZedBoard. Vivado is an IDE that comes with all the necessary software components to deal with the FPGA Register Transfer Level (RTL), synthesis, place and route, and configuration processes. It additionally includes the Software Development Kit (SDK) tool to handle all the 'C' software, operating systems, and other application software options available to be executed by the ARM microprocessor. Another significant task that Vivado accomplishes is the automatic creation of all the required interconnections between the FPGA and the microprocessor and its peripherals.

VNC servers were installed to allow the participants worldwide to remotely access a complete laboratory workstation as if they were physically in the ICTP facilities. A public IP address was given to each computer and personal credentials were provided to all the participants to access the VNC server through the 5900 port. Nevertheless, a second VNC server was also enabled to which only the laboratory tutors had access, with a common user-password for all the computers and mapped to the 5901 port. This allowed the tutors to connect to any of the participant's workstations when there was a need for specific assistance during the execution of the practical exercises. Likewise, an SSH server was also installed to obtain administrator access by the tutors to all the workstations without interfering with the activities carried out by the participants.

The web-based video conferencing service *Zoom* was used as support software for oral presentations, virtual group attendance, laboratory explanations, and general assistance. Throughout the presentations, the participants were encouraged to engage with questions in the *Chat* of *Zoom*. Furthermore, for laboratory sessions, the participants were organized into smaller groups. As a result, each group had a *Zoom Breakout Room*, which facilitated interaction between peers as well as with the designated laboratory tutor.

Once the time scheduled for the laboratory was finished, the participants were still able to keep working on their exercises, by remote access, and more significantly, they could still communicate among themselves as well as with the laboratory tutors by the use of *Slack*, a well-know communication platform. Therefore, whenever there was a doubt or question, it was possible to raise the inquiry to all the participants and tutors, promoting their interaction and pro-activeness.

In all the workstations, the in-house Universal Direct Memory Access (UDMA) [37] command-line interpreter (CLI) application (explained in Section 3.2) was also installed and, together with the VNC Client, was the only required software that the participants were asked to install in their own computers.

3.1.3. Resources Sharing Services

GitLab [38], a collaborative development platform built on the version control system Git, was used as a shared space between participants and instructors. The tools provided by GitLab include online storage for repositories, access control, and wikis.

For the remote laboratory, a public repository with a Wiki was created and special permissions were granted to the collaborators to edit the Wiki and to upload and modify files of the repository. Material such as the PDF version of the laboratory guides and the short presentation of each topic were uploaded to the repository as well as the source files for each laboratory session with their solutions. The school's wiki pages were organized into three categories: Laboratory Guides, Projects Guides and Support Documentation (software installation and how to access a remote workstation), shown as sections in the wiki index [39].

Additionally, a specific laboratory activity was proposed to the participants on how to use Git with Vivado projects and how to take advantage of code collaboration by using GitLab. Based on the guidelines provided by Xilinx [40] and the MLab team experience, a session was built around how to setup Vivado projects inside a local Git repository and how to upload it to GitLab.

3.2. In-House SoC-FPGA Development Framework

Given the complexity of the remote laboratory activities and projects and the limited allocated time for this online school, a development framework was provided to help the participants to focus their efforts on the central aspects and main topics of the school.

This development framework was proposed as a base design for advanced SoC-FPGA project implementations, and it includes the following in-house tools:

- The Communication Block (ComBlock) [41], which is an easy-to-use link layer between the microprocessor and the FPGA.
- The UDMA, a software application to encapsulate the interaction between the microprocessor and a personal computer.
- Hardware controllers that act as an interface between external devices and the user's core FPGA design.

All in-house tools were hosted in Gitlab and distributed under an open-source BSD-3 license. The integration of the ComBlock, the UDMA, and the hardware controllers defines a flexible development framework in which the participants create custom applications by adding their core FPGA designs and the application-specific software without having to deal with complex interfaces.

The whole design of the SoC-FPGA was developed in such a way to clearly separate predefined common services and free user design space [42], as shown in Figure 5. A brief description of these predefined blocks is provided below.

(a) *External Hardware Controller*: Provides a simplified communication interface between the instrument-specific FPGA design (Core FPGA design) and the time-critical external hardware, like the high-speed ADC500 DAQ mezzanine card described in Section 3.1.1. This functional block takes care of all the details of the configuration and handling mechanism of the external hardware.

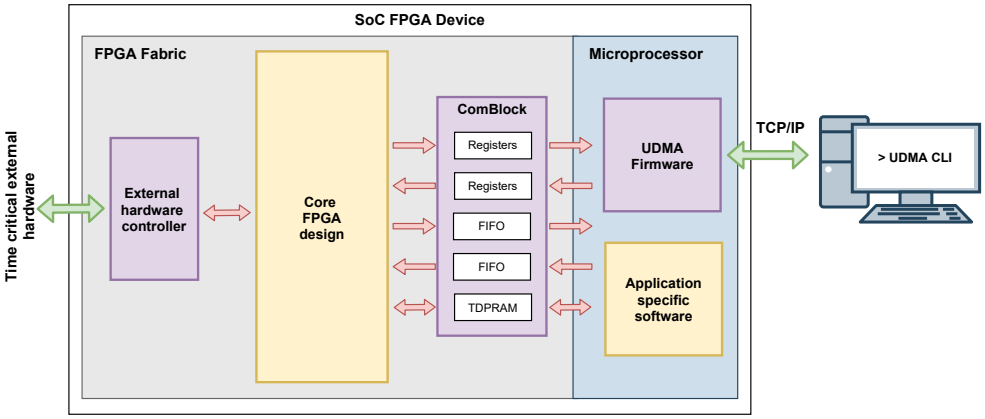

Figure 5. Block diagram with the main components of the SoC-FPGA of the experimental hardware platform. The purple boxes are the provided common services, and the yellow boxes are the user's free design and programming areas.

(b) *ComBlock*: It is comprised of three different memory elements that can be asynchronously accessed from both parts, the microprocessor software/firmware and the core FPGA design. The ComBlock contains input and output registers, two First-In-First-Out (FIFO) memories, and a True Dual-Port Random Access Memory (TDPRAM). The memory elements are accessed from the side of the FPGA using native interfaces, and from the microprocessor side through the SoC AXI bus [43]. Utilizing these three types of memory elements, all data exchanges between the FPGA and the microprocessor are covered. From the microprocessor perspective, user instantiated cores in the FPGA become memory-mapped peripherals for reading and writing operations.

(c) *UDMA Microprocessor Firmware*: It is a C library that provides functionality for a transparent communication channel between the ComBlock and a control computer. This firmware allows to exchange data, error messages, and configuration parameters between the computer and the core FPGA design or the application-specific software by means of predefined packets. It is implemented as an independent task in the underlying real-time microprocessor operating system (FreeRTOS), which supports running multiple tasks. TCP/IP over Ethernet was chosen to communicate with the computer either in a local area network or through the Internet.

(d) *UDMA CLI*: This is a user-friendly Python-based CLI running on the control computer. It provides a set of commands to interact with the SoC-FPGA. These commands allow reading and writing the memory resources of the ComBlock for interaction with the FPGA design. Given that the CLI was built on Python, it has the advantage of multi-platform compatibility, which allows users to install the UDMA CLI on their personal computers with ease. Another advantage is that these commands can be written sequentially in a file to create automation scripts to simplify the communication with the SoC-FPGA.

3.3. Laboratories and Project Activities

One of the goals of the school was for each participant to gain enough knowledge to develop their own projects once the school was finished. To facilitate the learning process, a series of experimental laboratories building on each other was prepared. Thereby, the laboratories began with the well-known basic 'Hello World' and progressed through a succession of in-depth exercises, including input/output interfaces, interrupt hardware and software, Direct Memory Access (DMA), development of a custom Intellectual Property (IP) module, and mastery of the ComBlock. As a final step of each laboratory, the designed system was implemented in a SoC-based development kit (ZedBoard) through the available remote access. For each laboratory, a detailed guide was elaborated to facilitate the understanding of the complex process of working with both the microprocessor and the FPGA at the same time. The laboratory guides are readily available on the school website. At the end of these laboratories, the participants were adequately prepared to face the challenge of the two final projects.

3.3.1. Project 1: Digital Pulse Processor for X-ray and Nuclear Spectroscopy

The purpose of this project was to develop a complete data acquisition and pulse processing system, based on the hardware setup described in Section 3.1.1. The system acquires and digitizes pulses coming from a detector, extracts their arrival times and amplitudes, and transmits the resulting data to a computer via Ethernet for offline energy spectrum analysis [44].

To simplify the design of the system, the project was divided into four laboratory activities, as follows:

1. *Data Acquisition*: This laboratory was focused on high-speed data acquisition and signal conditioning using the DAQ card introduced in Section 3.1.1. The analog signal coming from the detector was digitized by the ADC500 of the DAQ card. Then, the resolution of the signal was enhanced through a decimation block to get it ready for the DPP module. To test the design, a periodic analog signal with known frequency was generated with the Dig-AD2 instrument. The digitized data was read through a serial connection to a plotter. The participants adjusted the ADC500 parameters and the decimation factor to condition the signal for the final step of the project.
2. *Digital Pulse Processing*: The laboratory was centered on the implementation of a digital pulse processor on FPGA. The first part of the laboratory was dedicated to preparing a test environment by implementing a simple DPP to obtain the time of arrival and the amplitude of square pulses. The second part of the laboratory used the previous test environment to process typical PMT pulses from an experimental data set. The data were fed to the DPP by the microprocessor through the ComBlock.

3. *Data Transmission*: This laboratory was concentrated on the exchange of data between the SoC-FPGA hardware and a control computer using the UDMA in-house tools described in Section 3.2. Specific logic blocks were implemented to interact with the FPGA design through the ComBlock from the UDMA microprocessor firmware and the UDMA CLI running on the computer. As a result, data moving experiments were performed using the CLI commands from the laboratory workstation over Ethernet. Moreover, the UDMA CLI also allowed the participants to directly interact with the experimental hardware setup from their personal computers over the Internet.
4. *Project Integration*: This final laboratory integrated the previous three designs into a single project, completing the chain from the detector's data acquisition to the readout of the processed data on a computer, where the amplitude of the pulses were organized into a histogram to obtain the energy spectrum. Because of the limited number of PMT detectors, the participants initially tested their designs using synthetic pulses generated by the Dig-AD2 instrument. The detector was connected by the tutors on-demand of the participants for final testing of the system and for taking measurements of the background radiation.

3.3.2. Project 2: Data Acquisition System for Radiotracer Techniques in Environmental Monitoring

The goal of this project was to guide participants through the development of the firmware for the radiotracer system described in Section 3.1.1. The system periodically collects radiation spectra or counts pulses with amplitudes that fall inside a certain interval of values.

The presented system contained the following four main custom design blocks implemented as ready-to-use IP cores:

1. Embedded MicroBlaze processor core, which facilitated user access to design registers and data transfer to the computer.
2. Oscilloscope core for capturing data streams at outputs of different design blocks.
3. Signal conditioning core, which stabilized a possible slow varying DC level of the input signal, shaped exponential input signal with a finite rise and a fall time into a trapezoidal signal with predefined peaking time (with using a simple recursive algorithm) and stabilized a baseline that might fluctuate in case of a high counting rate (baseline restorer).
4. Pulse Height Analysis (PHA) core, which included: a (a) PileUp Rejector (PUR) for rejecting pile-up events; (b) timers for triggering a series of measurements; a (c) Peak Detector (PKD) for detecting pulses and measuring their height; and a (d) Multi-Channel Analyzer (MCA) for sorting pulses by their height into a dual-port memory.

The participants followed instructions and properly connected design blocks. Before each exercise, the functionalities and underlying algorithms implemented in the custom IP cores were explained by the tutors. When developing embedded processor applications, two methods were proposed: (1) Importing ready-made modules in each step of the design process, and (2) modifying source code from the previous steps according to written instructions.

3.4. Remote Laboratory Implementation Costs

The main costs to implement a remote laboratory are essentially related to human resources. A moderate cost contribution is represented by the specific hardware experimental platforms dedicated to the laboratory activities. These platforms are usually commercially available and their cost, tightly related to the performance, varies within a wide price range, from tens to hundreds of USD each. Since the purpose of most schools and training activities is teaching fundamental concepts and key design methodologies, it is not strictly necessary to perform experimentation on costly hardware. For experimentation on SoC-FPGA technology, it is possible to count on platforms costing about a hundred USD. These relatively cheap platforms essentially offer all key aspects found on devices whose cost could easily exceed thousands of USD. Moreover, these platforms can be shared

by several participants with access at different time slots. Most of the necessary standard equipment and services are nowadays available in many universities and research centers in most countries. While standard personal computers are widely available and internet connection is ubiquitous, this is not the case for the necessary ad hoc software tools and specialized technical support. Setting up a dedicated network of PCs that can be remotely accessed taking into account all potential threads requires expertise and specific skills of permanent staff in charge. The production of dedicated software solutions to remotely interact with the experimental setups requires long developing times and extensive tests to grant reliability and easy utilization. Another time-consuming task is the production of good quality documentation including introductory material, manuals, didactic guides, demos, and tutorials. Although the production of these materials requires a great effort, they can be easily reused and adapted to similar future activities.

4. Results

To receive feedback on the school and the remote laboratory, and to assess the level of satisfaction of the participants, the latter were invited to deliver final oral presentations and to complete a survey on the lectures and practical activities.

4.1. Participants' Presentations

On the last day of the school, the participants were encouraged to deliver an oral presentation with two main objectives: explain how they were able to successfully carry out the development of the proposed final project activity and share their personal experience regarding the school. In five minutes, they presented a brief description of the project and the development of the implemented solution. After that, they presented which specific school activity they considered more relevant for their research, which new topics they had learned, which difficulties and challenges they had faced, the resulting personal improvements at the end of the school, and any other individual comments and suggestions. The final presentations were delivered by 60% of the participants, and they can be found in PDF format on the ICTP school's website.

It should be emphasized that in the oral presentations the participants expressed a common appreciation for the contents, selected topics, lecturers, and the practical part of the school. They certainly appreciated the opportunity of having a remote computer to work with, the access to cutting-edge software tools, and the possibility of experimenting with state-of-the-art hardware platforms. They also highlighted the personalized assistance given by professional experts in different subjects as well as the progressive evolution of the laboratory activities, from a basic 'Hello World' exercise to the development of real scientific instruments. Furthermore, it was highly appreciated that all teaching and laboratory material, including tutorial guides, source codes of in-house software tools, and projects, were shared in the public school repository.

4.2. Feedback Survey

The participants' experiences are important for the evaluation and further improvement of the online school and remote laboratory. Therefore, a 14-item survey was given to participants at the end of the school, with both graded and YES/NO responses to questions, and some open text answers. The survey was answered by 23 participants.

The responses were graded on a five-steps scale from 1 (Poor) to 5 (Great) in most of the questions, and from 1 (Very Easy) to 5 (Very Difficult) in just two questions (questions 1 and 6).

The participants were asked to rate the following aspects of the school:

Q1: Level of difficulty of the laboratories and project activities.
Q2: Presentations of the lecturers.
Q3: Overall school activities.
Q4: Quality of the guides and the material received during the school.
Q5: Interaction with the laboratory tutors.

Q6: Complexity of the tools provided to interact with remote hardware setups.
Q7: Overall online experience during the school.

Figure 6 depicts the responses to the survey questions about the level of difficulty of the proposed practical activities (Q1) and of the use of the tools provided to interact with the remote experimental setups (Q6).

The majority of participants (56%) rated the proposed laboratories and project activities as *moderate level of difficulty*, while 30% rated the practical activities as difficult, and the remaining 14% rated them as easy. As for the use of the tools provided to interact with the remote hardware setups, over half (61%) evaluated the tools as *easy* or *very easy*, 26% as *difficult* or *very difficult*, and only a few participants (13%) as neither easy nor difficult.

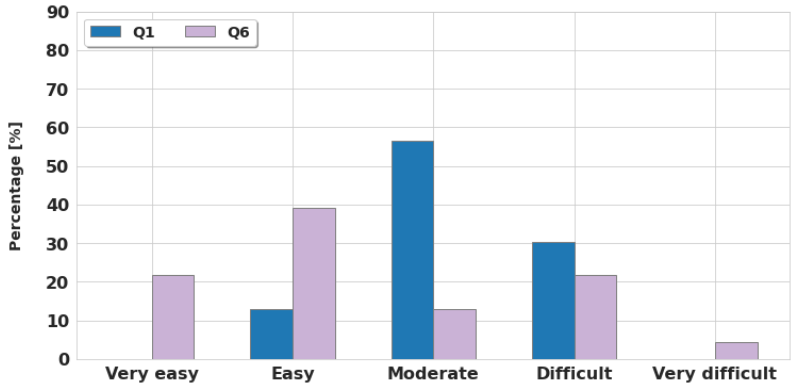

Figure 6. Survey responses to questions Q1 and Q6.

Figure 7 shows the responses regarding the presentations of lecturers (Q2), the interaction with laboratory tutors (Q5), and the quality of the material received during the school (Q4). The figure also illustrates the participants' responses on the overall school activities (Q3) and the overall online experience during the school (Q7).

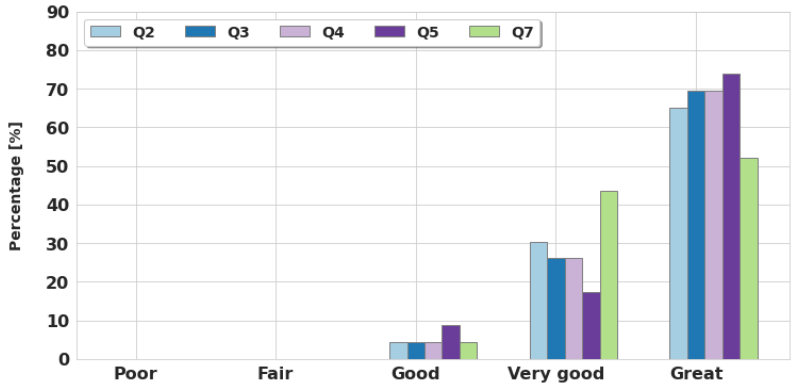

Figure 7. Survey responses to questions Q2, Q3, Q4, Q5, and Q7.

The results show that the absolute majority of the participants evaluated as *Great* or *Very Good*: the presentation of the lecturers (Great: 65%, Very-Good: 30%), the interaction with the laboratory tutors (Great: 74%, Very-Good: 17%), the guides and the material received during the school (Great: 70%, Very-Good: 26%), the overall school's activities (Great: 70%, Very-Good: 26%), and the online experience (Great: 52%, Very-Good: 43%); whereas only a few participants (one person in most of the cases and two people in only one case) rated them as good.

The YES–NO survey's responses were associated with optional open text comments. It was asked if they considered that:

Q8: The contents and selected topics of the school were appropriate.
Q9: The proposed online modality was effective and efficient for the school.
Q10: The newly acquired knowledge will be useful for their future research or teaching activities.

It was also asked if they:

Q11: Did not come across any disruption of services to the online experience.
Q12: Would consider taking another similar school in remote mode if given the opportunity.

Figure 8 depicts the rate of the positive (YES) answers to the questions from Q8 to Q12.

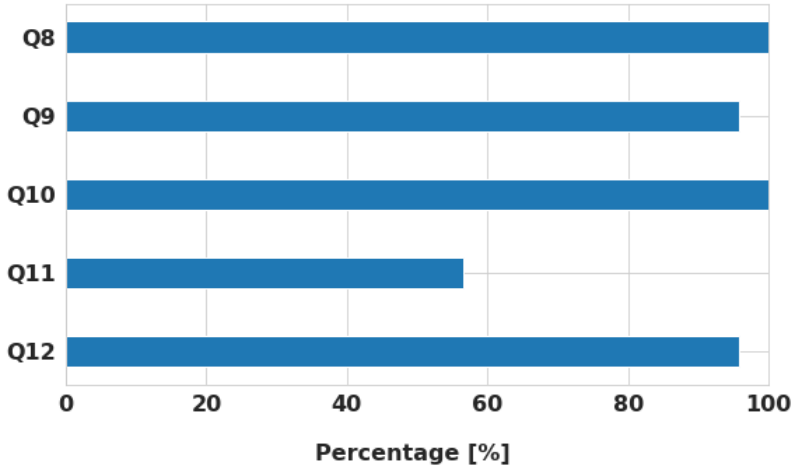

Figure 8. Positive responses to survey questions Q8, Q9, Q10, Q11 and Q12.

It should be highlighted that 100% of the surveyed participants considered that the contents and selected topics of the school were appropriate (Q8) and that the newly acquired knowledge will be valuable for their future research and training activities (Q10). Moreover, all the participants, except for just one, affirmed that the proposed online modality was effective and efficient for the school (Q9), and that they would take another similar school program in remote mode if given the opportunity (Q12).

In reference to Q11, considering the heterogeneous geographical distribution of the participants, it is remarkable that 56% of them did not come across any disruption of services related to the online experience, and the other 44% had sporadic network interruptions or electricity power cuts.

Finally, there were two optional open-ended questions regarding possible suggestions to improve the school and any other additional comments. Some of the free-text responses are included in the Appendix A.

5. Conclusions

Remote laboratories for advanced international training activities on fully programmable Systems-on-Chip and their applications to nuclear and scientific instrumentation pose several challenges well beyond the intrinsic complexity of the subject. The adopted strategy and tailored technical solutions were critical for achieving the School's goals while overcoming these three main difficulties: (i) Enabling remote access and full control of complex hardware platforms and experimental setups; (ii) providing real-time supervision and assistance on all phases of the programmed activities; and (iii) allowing efficient collaboration among participants to achieve the objectives of the proposed team-based projects in a very limited time.

The proposed design environment based on predefined common services has been proven effective in shortening development times of instrumentation based on SoC-FPGA platforms. This approach has also strengthened the collaborative working activity by allowing a seamless contribution from participants with different skills and backgrounds. Likewise, it has also allowed the laboratory tutors to provide efficient remote assistance

to the participants not only in the proposed laboratories, but also in all the phases of the proposed final projects.

The outcome of the participants' survey and oral presentation was extremely positive. The survey findings indicate that all participants gained new practical knowledge and skills that would be beneficial in their future activities. They were also highly satisfied with the online methodology and topics covered by the school.

The entire teaching and laboratory written material being shared with all participants and the open source approach were also greatly appreciated. Therefore, it can be affirmed that the overall remote laboratory experience, with participants accessing it from all around the world, was definitely successful.

Author Contributions: Conceptualization, M.L.C., F.F., A.C. and M.B.; methodology, M.L.C., F.F., A.C., M.B., C.O. and C.S.; software, C.O., C.S., R.M. (Rodrigo Melo), W.F.S., R.M. (Romina Molina), L.G.G.O. and B.V.; validation, M.L.C., F.F., A.C., M.B., C.S., R.M. (Rodrigo Melo), W.F.S., R.M. (Romina Molina), L.G.G.O. and B.V.; investigation, M.L.C., F.F., A.C., M.B., C.S., R.M. (Rodrigo Melo), W.F.S., R.M. (Romina Molina), L.G.G.O. and B.V.; resources, M.L.C., F.F., A.C., M.B. and C.O. writing—original draft, M.L.C., F.F., A.C., M.B., C.S. and C.O.; writing—review and editing, M.L.C., W.F.S. and A.C.; supervision, M.L.C., A.C., F.F. and M.B.; project administration, M.L.C. and F.F.; funding acquisition, M.L.C. and F.F. All authors have read and agreed to the published version of the manuscript.

Funding: This activity was funded by the Abdus Salam ICTP (UNESCO) and IAEA.

Acknowledgments: The authors thank the support of the ICTS team of ICTP and the school's secretaries, Monica Ancuta, Viktoriya Lvova, and Adriana Pinto, for their excellent administrative and technical support in all phases of the activity.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

AFE	Analog Front-End
CET	Central European Time
CLI	Command-Line Interpreter
DAQ	Data Acquisition
DHCP	Dynamic Host Configuration Protocol
DMA	Direct Memory Access
DNS	Domain Name System
DPP	Digital Pulse Processing
Dig-AD2	Digilent Analog Discovery 2
FIFO	First-In First-Out
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
HLS	High Level Synthesis
HV	High Voltage
IAEA	International Atomic Energy Agency
ICTP	International Centre for Theoretical Physics
IDE	Integrated Design Environment
IP	Intellectual Property
MCA	Multi-Channel Analyzer
MLab	Multidisciplinary Laboratory
NSIL	Nuclear Science and Instrumentation Laboratory
PHA	Pulse Height Analysis
PKD	Peak Detector
PMT	Photo-Multiplier Tube
PUR	Pile-Up Rejector

PoE	Power over Ethernet
RTL	Register Transfer Level
SDK	Software Development Kit
SSH	Secure Shell
SoC	System-on-Chip
TDPRAM	True Dual-Port Random Access Memory
UDMA	Universal Direct Memory Access
UNESCO	United Nations Educational, Scientific and Cultural Organization
VNC	Virtual Network Computing

Appendix A

Some participants' free-text responses from the survey:

"It would have been useful to post the solutions to all projects and exercises."

"Some preliminary online modality tests for self-checking could be very useful."

"Some lectures were interesting but took too much time of the main aim which was the practical knowledge on the SoC-FPGA hardware boards."

"This school was the best. Other events need to learn how to conduct lab activities."

"My suggestion would be to multiply more activities like this and give the opportunity to as many people as possible to benefit from it despite the limited resources."

"Conducting practical sessions online is a huge challenge. ICTP perfectly managed those things."

"It was great to have a computer to work with remotely. I enjoyed the labs because they were practical. I enjoyed the lectures because they went beyond just information to give the "why" behind things."

"Experience Gained: Developed my first SoC application. Started learning to use an OS on an embedded system. Built my first IP (IP-demystified: IPs are not written only by Martians). Got a better understanding of Git."

"I applied for this school in order to learn and gain experience in SoC for instrumentation. I have gotten more experience than I desired. I am already planning exercises that I will use with my students next semester."

"Most fruitful event attended in the pandemic. Best school with excellent lab activities with the best faculty."

"The fact that this training was online made it possible to go beyond the planned objectives because, in addition to the knowledge related to FPGA and SoC, we were able to use different e-learning tools that further enrich the school's program."

"I learned so many new things. Using hardware remotely was an experience that needs to mention lab tutors' wonderful expertise."

"I really liked the possibility of remote access to the development hardware board."

"Thank you so much to the organizers, all the amazing tutors, and incredible professors. I'm so grateful for being part of this school."

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