Design and Performance of Data Acquisition and Control System for the Muon g-2 Laser Calibration

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***Abstract*— The Muon g-2 Experiment at Fermilab (E989) will measure the muon magnetic anomaly with unprecedented precision (0.14 ppm), which yields a factor of 4 improvement with respect to the previous measurements at Brookhaven National Laboratory (BNL) (E821). To achieve this goal, the relative response of each calorimeter channel must be calibrated and monitored at a level better than 10^{-3} in the time window of the muon fill. The calibration system uses a laser source and photodetectors. The data acquisition (DAQ) of the system is designed around two field-programmable gate array (FPGA)-based boards and a custom crate bus. The front-end board manages the photodetector operation and signal processing and performs a first-level data concentration task. Up to 12 FPGA boards can be housed in a 6U crate. A readout master controls the boards, implements event-building functionalities, manages the monitoring interface, and facilitates calibration and debugging tasks. A gigabit-ethernet interface is used to transfer data to the on-line farm for storage and further processing. Presently, the system is working at Fermi National Accelerator Laboratory (FNAL). In this article, we present the DAQ system design, run control user interface, and system evaluation.**

***Index Terms*— Calibration system, data acquisition (DAQ) and control, field-programmable gate array (FPGA).**

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I. Introduction

LASER calibration systems of experimental facilities in high energy physics (HEPs) are widely used to provide precise energy and timing references to various subdetector elements. In addition, laser devices are key elements in the control and monitoring systems of detectors and readout electronics. In fact, the possibility to mimic physics events by means of a laser beam allows the study of the detector response, the validation of trigger procedures, and the exercise of the data acquisition (DAQ) system.

When high-speed applications are not needed, the processing activities of sensor nodes can be performed by a digital signal processor (DSP) or programmable microprocessors. On the other hand, field-programmable gate arrays (FPGAs) are preferred in cases where real-time processing is desired. This is due to the flexible architecture, which provides highly parallel custom resources.

In this article, we present the DAQ and control system for the state-of-the-art laser calibration facility of the Muon g-2 experiment [1]. The goal of the E989 experiment is to measure the muon magnetic anomaly, $a_\mu = (g_\mu - 2)/2$, to a precision of 16×10^{-11} (0.14 ppm, statistical and systematic). A polarized beam of positive muons is injected and stored inside a ring with a highly uniform magnetic field of 1.45 T. The spin precession frequency ω_a is extracted by measuring the modulation of the rate of higher energy positrons from muon decays, detected by 24 calorimeter stations placed equidistantly around the inner radius of the storage ring. Each station consists of an array of 6×9 PbF_2 crystals instrumented with a matrix of SiPMs to detect the Cerenkov light produced by the positrons and provide a precise energy reconstruction [2]. A 12-bit waveform digitizer (WFD) samples each calorimeter signal at a rate of 800 MSPS, and the data are transferred to a bank of GPUs for on-line data processing.

II. Calibration System

In order to achieve a systematic uncertainty of 0.07 ppm, the calorimeter detectors need a reliable and accurate

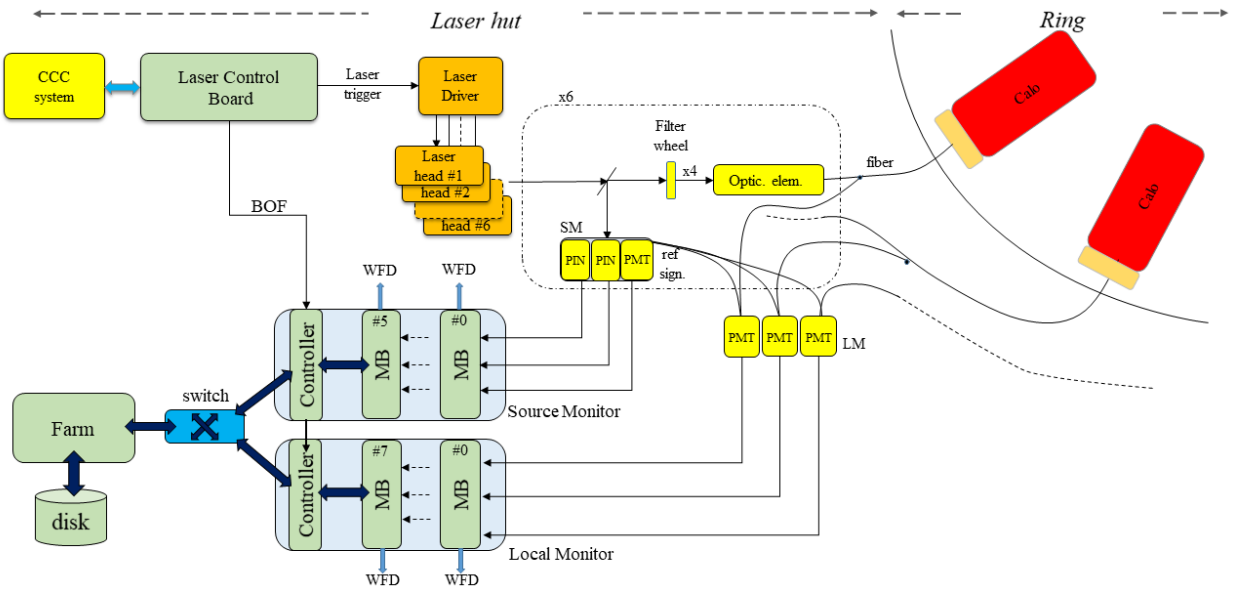

Fig. 1. Schematic of the calibration system for the Muon g-2 experiment. The photodetectors of SM and LM systems with front-end electronics and DAQ system are hosted in the laser hut.

calibration procedure. The uncertainty associated with the gain fluctuations, which affect the ω_a measurements, must be limited to sub-per mil level during the muon decay time scale (0–700 μs) and to sub-per level in between fills and over the longer period. The calibration method is to distribute synchronous laser pulses, having the same SiPM response as for those produced by positron showers, directly into each of the 1296 crystals.

A sketch of the distribution system is displayed in Fig. 1. The light pulses are generated by six identical diode laser heads with a maximum pulse energy of 1 nJ and a pulsewidth of about 700 ps (at 405 nm). The laser light of each line, sent through a filter wheel and a beam splitter, feeds four quartz optical fibers (about 30 m long). The light of each fiber is delivered to a diffuser to achieve beam uniformity before a bundle of polymethyl methacrylate (PMMA) (acrylic) fibers distributes the light to 54 calorimeter crystals. More details regarding design, implementation, and test results of the light distribution system can be found in [3]. As shown in Fig. 1, the light of the distribution system is monitored twice along the optical path by several photodetector elements both immediately at the beam exit and at the end of chain near the calorimeter crystals. The first element is called the source monitor (SM) and uses about 30% of the laser light. It is based on an integrating sphere and a redundant system, made by two large-area p-i-n diodes (PINs) and a photomultiplier (PMT), to monitor the stability of the laser source. The PMT is also coupled to a radioactive source (Americium-241) whose alpha particle passage into a scintillator provides an absolute reference light source. The second component, called the local monitor (LM), was designed mainly to monitor the stability of the light distribution system. Two fibers in each bundle carry light signals back to two PMTs in the Laser Hut, from which the LM acquires data. A reference signal coming from the SM is provided to each PMT of the LM.

The total number of photosensors of the calibration system is 66 (18 and 48, respectively, for SM and LM). The two monitors deal with distinct signal characteristics as the pulse energies at the monitoring points span several orders of magnitude (i.e., from hundreds of pJ for SM to a few tenths of pJ for LM), requiring different signal processing electronics. The redundancy in the SM and LM systems is needed to monitor and compensate any fluctuations due to both the laser source, optical distribution system, and so on, and due to the gain variation of the photodetector or temperature instabilities.

III. DAQ Architecture

A specialized electronics module monitoring board (MB) has been designed to manage signal processing and data readout for SM and LM channels. In fact, the LM channels are divided into two groups of 24 and acquired by MBs and WFDs, respectively. The DAQ architecture consists of two custom crates hosting MB modules and a master board (Controller) [4] which performs a trigger-driven data collection, operates as an event-builder, and transfers data to the online farm. Good linearity in the front-end electronics, capability to manage different types of photodetectors by means of an embedded control and monitoring system, and online processing to provide calibration factors are the main features of the DAQ.

The calibration data flow is driven by the laser firing program, defined in the laser control board [5] that manages the interface between the calibration system and the experiment's synchronous control system, the clock and control center (CCC). The muon beam cycle consists of 16 subcycles divided into two groups of eight separated by about 200 ms. Each subcycle contains a 700-μs window called "in-fill" (characterized by the muon decays) and the "out-of-fill" window of about 10 ms. The injection cycle repeats every 1.3 s. Each subcycle, the basic time slot for data assembling, lasts about 10 ms. The laser control board provides the begin-of-fill (BOF) signal to the Controller that represents the beginning of the subcycle time slot.

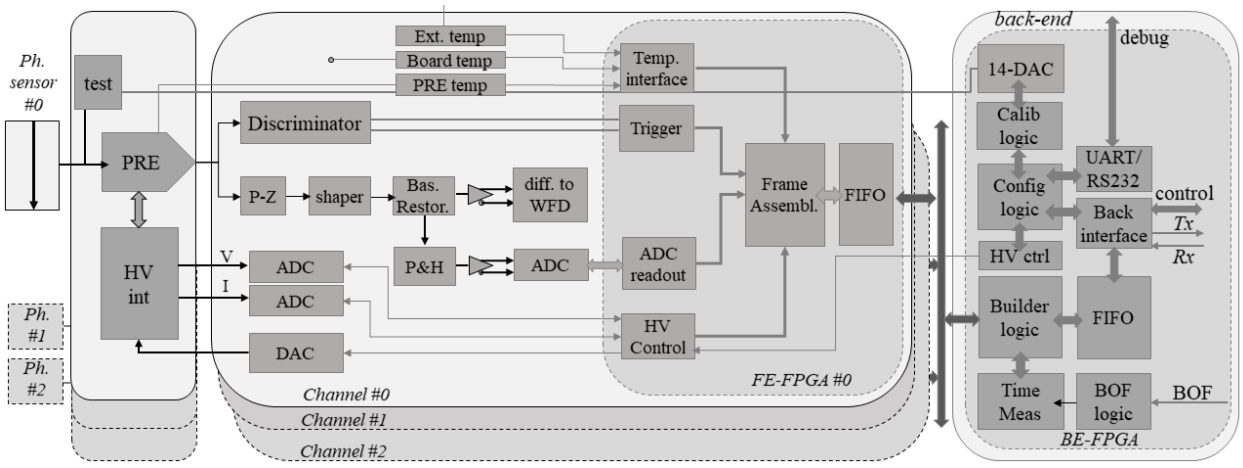

Fig. 2. Schematic block diagram of the front-end electronics and MB processing chain.

The laser can be operated in two distinct modes concerning physics or test runs. During physics runs, the generation of laser pulse trains occurs during both the "in-fill" (superimposed to the positron data) at a typical rate of 10 kHz and the "out-of-fill" time windows. The second mode is devoted to the test runs without beam in order to exercise the DAQ and detector according to the exponentially decreasing time function, $e^{-t/\tau}$, which is expected in the experiment due to muon decay. The average number of laser hits generated in this mode is about 100. Then, considering the two modes, the expected values of laser pulses $\langle N_{\text{pulse}} \rangle$ per subcycle should not exceed 100.

A. Preamplifier

A typical photodetector response to the laser pulse produces an electrical signal whose charge is proportional to the input light intensity. In order to optimize the signal-to-noise ratio (SNR), the signal is integrated, amplified, and then filtered. The amplification stage strongly depends on the sensor characteristics (i.e., the sensor capacitance and the dark current). The preamplifier, used to amplify the photodetector signal, was installed on a daughter board placed at 3 m from the MB front-end panel. This facilitates a custom and flexible interface with the sensor. The basic circuit has been optimized based on the photodetector type in the SM and LM. The PINs, used in the SM, are Hamamatsu S3590 [6] series operated with a 50-V reverse bias to reduce the response time and junction capacitance (the output capacitance with this bias voltage is about 40 pF). On the other hand, the dark current increases with the reverse voltage (about 2 nA with a 50-V reverse bias). The use of a PIN requires a high operational gain and a careful design of the amplifier.

The front-end electronics are based on a charge sensitive preamplifier ("PRE" in Fig. 2). It has been specifically designed to efficiently acquire the signal from the PIN device whose charge produced from a laser pulse is expected to range from 1 pC to a few pC with a rise time of about 10 ns and a fall time of hundreds of nanoseconds. The adopted configuration is based on a classical scheme reported in [7] with a cascode configuration with a feedback capacitor of 1 pF in parallel with a resistor of 10 MΩ. The conversion gain of the preamplifier is set to about 800 mV/pC to correctly dimension the operative range.

The chosen PMT for the SM signal is also manufactured by Hamamatsu (H5783-04 model) [6]. It is a metal package PMT with an integrated high-voltage power supply circuit. The control voltage applied is about 0.7 V corresponding to a typical gain of 10^5. The PMT produces a larger charge signal and a faster response than the PIN signal. The rise time is about 5 ns, and the fall time is 30–40 ns providing a roughly 50-mV pulse over a 50-Ω termination. The corresponding preamplifier circuit adopts the same scheme as for the PIN but with a conversion gain of 7 mV/pC. This value has been tuned to efficiently acquire both the laser and Americium signals. The last configuration has been optimized for the LM signal from Hamamatsu R1924A PMT [6] whose shape characteristics are comparable to the PMT of the SM.

In the daughter board, a test capacitor of 1 pF is at the input of the preamplifier. Here, we can test the on-board calibration without the photodetector signal (see later in this section) by applying a charge injection (test signal). The low voltages (+12, −12, and +5 V)—that the preamplifier needs—are provided by an MB through a flat cable that distributes the test signal too. The output of each preamplifier feeds the corresponding MB input channel via a coaxial cable.

B. Monitoring Board

The MB contains three input slices for processing photodetector signals. A schematic block diagram of the MB is depicted in Fig. 2; the picture of the module is shown in Fig. 3. The MB processing does not require any external trigger. In fact, each channel is self-triggered and when the preamplifier amplitude is greater than the threshold (Th1), a fast trigger is generated and the pulse will be acquired. The use of a threshold selectively removes very small signals. A second threshold (Th2, with Th2 > Th1) allows the discrimination between laser and Americium signals.

The long tail which characterizes the output of the preamplifier has been removed by a pole-zero ("P-Z" in Fig. 2) cancellation circuit based on a filter with a capacitor of 330 pF.

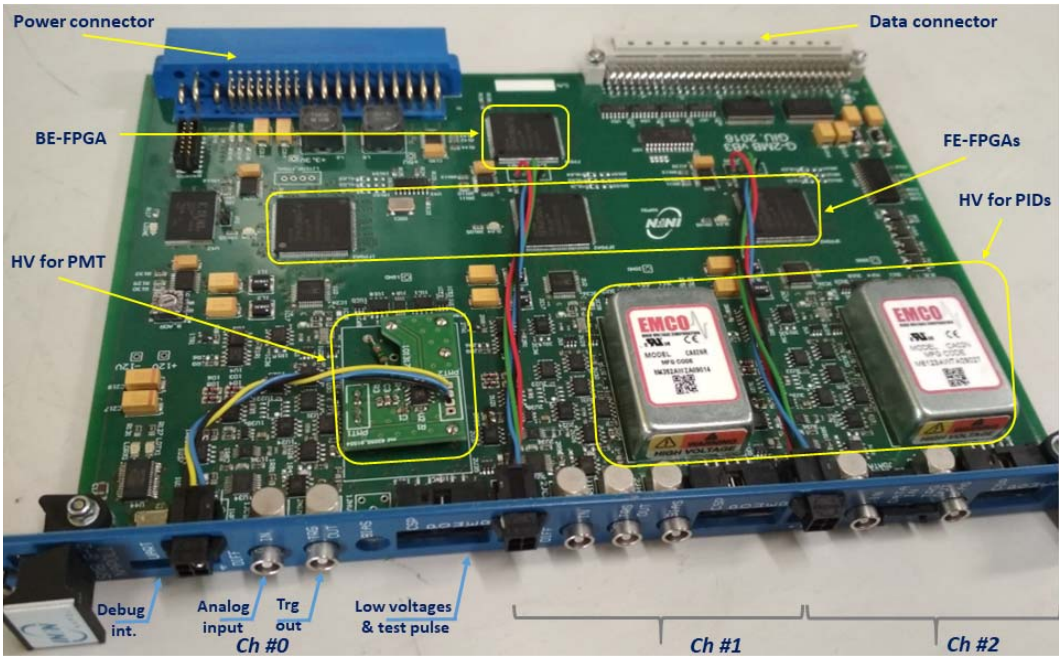

Fig. 3. Picture of the MB with a setup that manages three SM photodetectors (two PINs and one PMT).

Pole-zero cancellation filter avoids the pile-up effect. In the stage that follows, the pulse shaper circuit is based on a high-pass filter followed by low-pass filters (CR-nRC shaper). The analog components of this circuit have been chosen to obtain a pulsewidth of 600 ns. It is worth mentioning that an excessive reduction of the pulsewidth makes the SNR worse. The baseline restorer is the next element in the analog chain; it avoids the baseline shift causing uncertainty in the peak determination. This dc offset is generally caused by the amplifier gain with a unipolar signal in the case of a high-counting rate. The adopted scheme allows the pulse rate to reach 20–30 kHz, beyond the expected rate. The output of the baseline restorer feeds a peak and hold logic that is composed of an amplifier charging a capacitor through a diode. The scheme includes a reset signal, which is normally asserted, allowing the output voltage to follow the input by means of a fast capacitor discharge. When a trigger pulse is generated by the discriminator and trigger logic, the reset will be removed during the acquisition gate. In this configuration, the circuit is able to keep the highest reached value with a voltage drop rate contained within 30 μV/μs, which does not introduce systematic effects. The output of the peak and hold stage is converted into a differential signal and sent to the input of an analog-to-digital converter (ADC) device. Specifically, we use the AD9244 from Analog Devices, which has a 14-bit accuracy and sustains up to 65 MSPS data rates [8]. The ADC operates continuously, samples the input signal at a rate of 40 MHz, and stores the data in a circular buffer implemented in the "ADC readout" block of the front-end FPGA (FE-FPGA).

With the arrival of a trigger pulse, in order to register the baseline value, the "ADC readout" logic transfers up to 16 consecutive samples pertaining to the baseline measurements from the circular buffer and averages the value. After a delay of about 600 ns with respect to the trigger pulse, which guarantees the stabilization of the highest value of peak and hold, the "ADC readout" logic collects 16 new samples from the buffer in a 400-ns time window (16 clock cycles at 40 MHz) and calculates the corresponding average value of the peak. The "Frame Assembling" block (depicted in Fig. 2) builds a data packet for each pulse (validated by a trigger) composed of a header with trigger and BOF numbers, slow control information, and a block with five words of 16 bits containing pulse information (i.e., americium, laser, calibration, and simulation), timestamp (relative to the reference from the Controller board with a 10-ns accuracy), and baseline and peak words. The event data are stored in a local FIFO, implemented in the FE-FPGA, which allows buffering of about 1000 events ($\sim$32 kbyte, each event has 16 words). To monitor the FIFO filling and prevent the overflow condition, the status register is recorded in each frame. The back-end section of the MB will take care of the event building at the board level and data transfer to the Controller, as it will be described later on.

Each MB channel contains an embedded control system (hosted in the FE-FPGA) to set the high voltage by programming a dedicated 12-bit digital-to-analog converter (DAC). The effectively applied values can be readback and monitored by means of voltage and current measurements through dedicated ADCs, as shown in Fig. 2. The board includes three temperature sensors per channel: one on the module, another on the preamplifier, and the third, being detachable, can be placed in the surrounding environment. These sensors have an accuracy of 0.1 °C, essential to perform the gain correction. All the slow control measurements are available to the monitor system and can be attached to the data frame.

The last part of this section is devoted to the communication with the master for the data transfer. As seen, the MB performs DAQ processes based on two buffer levels allowing data decoupling between front-end readout and data transfer to the Controller. FE-FPGAs continuously acquire pulses and

store temporarily the data frames into the internal FIFOs. The "Builder logic" inside the back-end FPGA (BE-FPGA), initiated by the Controller board through the distribution of the BOF signal, reads the data frames from the three FIFOs, and performs the event-building at the board level. For example, all the three data frames for a given subcycle defined by the BOF number are unpacked, reassembled after a BOF-matching check, and pushed in the builder FIFO. The length of the data packet depends on the number of light pulses. Five 16-bit words correspond to each photodetector pulse, that is, 15 words/pulse per board. Moreover, the PMT counting rate is incremented by a small amount due to the Americium source with a 10-Hz activity. A header, containing 24 words with monitoring and control information, is attached to the frame. The reading process from the front-end FIFOs proceeds with a data rate of 16-bit word every 25 ns, and it will be completed (in case the FIFOs are full) within 1.2 ms, sustaining a peak pulse rate around 100 kHz (about 1000 events in a 10-ms subcycle time window). The expected laser pulse rate is about 10–20 pulses each subcycle in the standard laser program and can be increased to about 100 pulses/subcycle with the physics simulation mode which is still much lower than the sustained peak value. The depth of the builder FIFO hosted in the BE-FPGA guarantees the processing and storage of the input data flow for several subcycles. Once the reconstructed data are present in the FIFO, the transfer to the Controller can start.

The MB signal processing and data readout are fully handled at the hardware level. Except for the module initialization, the activities do not require any access. BE-FPGA hosts most of the internal registers to program the board and operates as a gateway to reach the internal resources. All the parameters can be set by means of the Controller through the backplane interface. The four FPGAs are from Xilinx (Spartan-6 XC6SLX9-2CSG324) [9]. Different versions of FPGA firmware, developed in a VHSIC Hardware Description Language (VHDL) code, allow the use of the same hardware platform to manage different photodetectors (i.e., SM and LM) diversified by means of the loaded configuration files. A 14-bit DAC (THS5671A, manufactured by Texas Instruments) [10] is also housed in the back-end section, allowing the electronics self-calibration.

C. Readout Controller

The Controller is a double-height board that acts as a master to handle the communications with the MBs. It manages all the phases of data taking, allowing the user to access the front-end electronics for configuration and monitoring. In particular, it performs the following.

1) Initialization of the MBs by means of the configuration registers hosted on the Controller.
2) Synchronization cycle of the BOF counters.
3) Readout cycle from each MB verifying the data frame consistency.
4) Event-building and data transfer to the farm server.
5) Slow control monitoring and electronics status logs.
6) Deliver each asynchronous command to the MBs both for configurations and monitoring purposes.

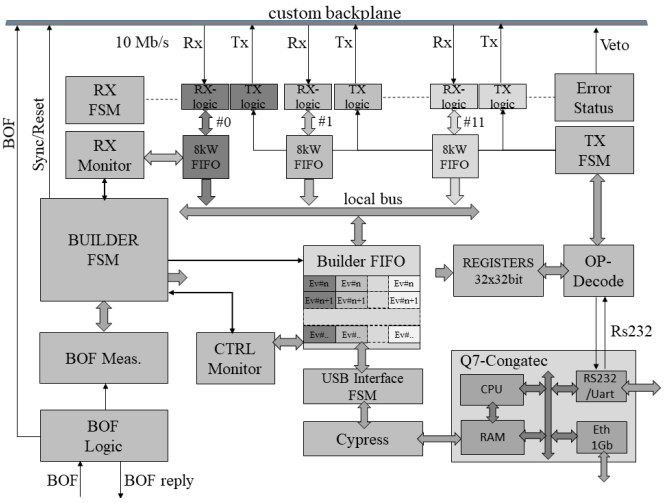

Fig. 4. Block diagram of the Controller board.

The communications and data transfer between each MB and Controller is accomplished by a custom protocol exploiting two reserved serial lines, realized on a monolithic backplane, implementing TX and RX interfaces inspired by the RS-232 standard [11]. The maximum number of MBs hosted in the crate is 12; a rotary switch is used to define the TX-RX geographical map. There are also some control signals that are broadcast by the Controller to the MBs in order to implement the readout protocol (i.e., BOF signal, synchronization/reset signals, veto).

The Controller is a single-board computer that integrates an Artix7 FPGA by Xilinx [12] and an Advanced RISC Machine (ARM)-based Qseven processor [13]. A block diagram of the board is shown in Fig. 4. The input section of the board has 12 identical slices to manage the incoming data flow from the MBs. The readout chain is based on a trigger-driven algorithm where all the MBs and the Controller share the same trigger signal (BOF) coming from the laser control board. When a BOF arrives, each MB operates the data assembling for the current BOF subcycle, as described in Section III-B and then transfers the data frame to the Controller (at 10 Mbit/s). The Controller reads in parallel all the MB frames pertaining to the same BOF, checks the data integrity, attaches several control words, and writes the reconstructed frames into receiver FIFOs. The use of a buffer memory improves the decoupling between the input and output sections. An RX monitoring logic is responsible for processing slow control data. When all the data packets from the MBs labeled with the same BOF number are completely written in the receiver FIFOs, the "BUILDER finite-state machine (FSM)" block starts the parsing of subframes and pushes them into the "Builder FIFO" until the last board is reached. The ARM-based processor takes care of the final readout by means of high-speed connections based on the Universal Serial Bus (USB) implemented by a Cypress FX2LP Microcontroller [14], which sustains up to 480 Mb/s. The logic to control the Cypress device is implemented in the "USB interface FSM" block. The data are then sent to the online farm through a gigabit ethernet connection for further processing.

Each MB, in the case of an error condition, occurred during the data taking, asserts the error line that propagates to the

backplane where it is gathered by a wired-OR logic and sensed by the Controller that promptly starts a debug cycle to latch the error condition. If an MB reaches the full FIFO condition, a busy signal is asserted, and the data taking is blocked until this state is lifted. The FIFO status flags are monitored and acquired during the data taking. Twelve "TX-logic" blocks are controlled by "TX FSM" to send commands and requests to the MBs. The "OP-Decode" logic processes the instruction words delivered by the embedded CPU and allows access to the corresponding resource (internal or external) by using a unique instruction format.

The calibration system for the Muon g-2 experiment consists of two crates: one for the SM and another one for the LM. The event-building at the crate level is fully realized at the hardware level, while the final event-building at the chain level must be implemented in the farm server.

D. Online Farm

The online farm consists of a PowerEdge R740XD Server [15] with AMD EPYC 7302P CPU (16 cores) running at 3.0 GHz. A total of 32-GB RAM is installed on the server. It is equipped with a total storage space of 8 TB configured in RAID1. The present configuration provides full redundancy for data processing and run managing that can be highlighted as follows.

1) Data receivers from the two Controllers.
2) Event-building and data storage processes.
3) Spy and decoding processes for slow control and monitoring.
4) The Run Control software that allows the user to manage the DAQ system for configuring/controlling the laser calibration system and the data taking.

The online processes are mainly distributed on four nodes in the DAQ network: the back-end node is represented by the online farm, while the two Controller CPUs and the laser control constitute the front-end machines. The Run Control offers a graphical user interface (GUI) to manage the run activity, monitoring network, and error logs. The online farm hosts a web server with several broad functions. It acts as a gateway for the laser system. It also serves as a database both for raw and processed data. For example, laser-firing configuration, photodetector peak amplitudes, baselines, slow control data, and the online monitoring data are also accessible.

IV. Test and Performance

This section reports on some tests carried out on the preamplifier and MB to verify correct linearity and processing. The assembly of all the DAQ components in the final configuration, the validation of the data collection, and the event-building performed by the Controllers are also discussed in this section. Finally, an example of how the Run Control accesses the online data and displays the monitoring information is provided.

A. Linearity Test

The first study concerns the linearity measurements of the charge-sensitive preamplifier. In our setup, a pulse generator (Agilent 33 250 with a 12-bit amplitude resolution) provided

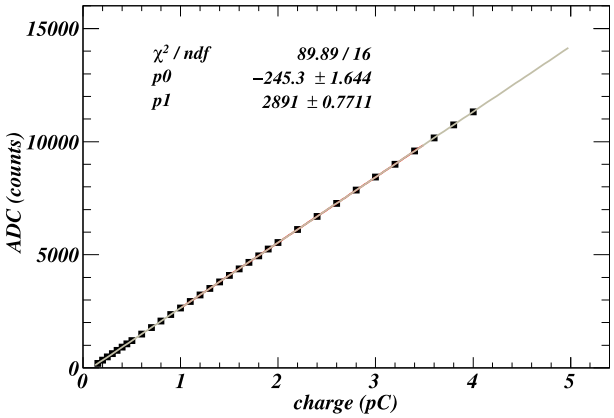

Fig. 5. Linearity measurements for the preamplifier performed with an MCA Canberra multiportII (14 bit).

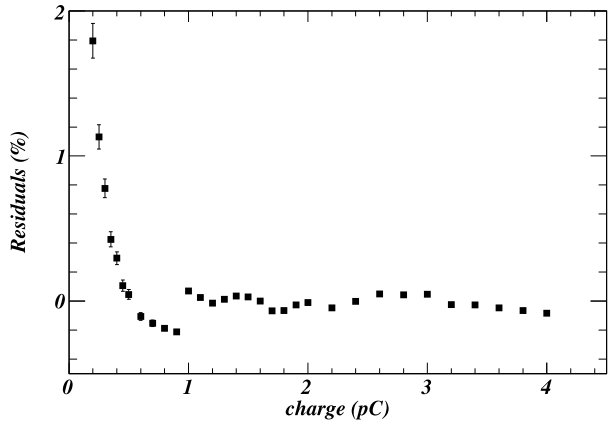

Fig. 6. Residuals with respect to a linear fit (measurements on the preamplifier board).

the charge injection into the preamplifier test capacitor by delivering a square-wave pulse. Voltage measurements were performed with a 14-bit multichannel analyzer (MCA) Canberra MultiportII [16] at the output of the preamplifier. For every value of charge, ranging from fractions of 1 to 4 pC, about one thousand voltage measurements were collected. The signal amplitude of the preamplifier versus the charge is shown in Fig. 5. A linear fit is performed on the measurement points in the charge interval 1–4 pC and the residual behavior is reported in Fig. 6. For a charge greater than 1 pC, the spread is within 0.1%. We conclude that the preamplifier has good linearity in the regions of interest, showing a deviation from linear behavior within 0.1%.

In order to perform automatic calibration campaigns for the three electronic chains of all MBs, an on-board calibration procedure based on a DAC has been implemented. To do that, a linear ramp generator, programed by software, has been realized in the "Calib logic" block of the BE-FPGA (Fig. 2). For example, the calibration mode, set by the Controller by means of a specific run, is defined in each MB as the sequence of ramps (number of waveforms, maximum, and step values) which is generated and distributed on the test capacitance as shown in Fig. 7. The ramp slope, defined by 1 DAC LSB over a 25-ns clock period, simulates the charge injection signal. During the calibration runs, the photosensors HV has been

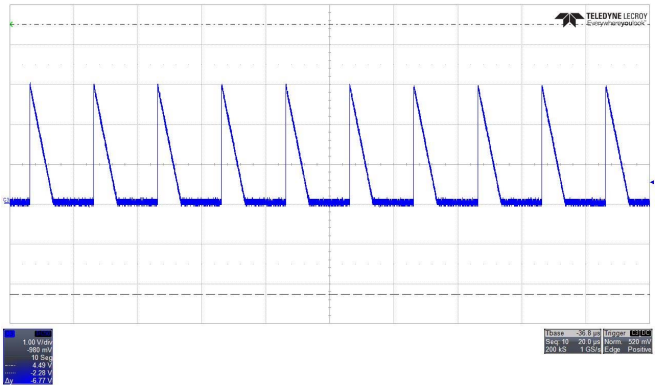

Fig. 7. Typical ramp sequence generated inside the MB and acquired by the oscilloscope. The maximum value is about 3 V with a step of ∼10 mV.

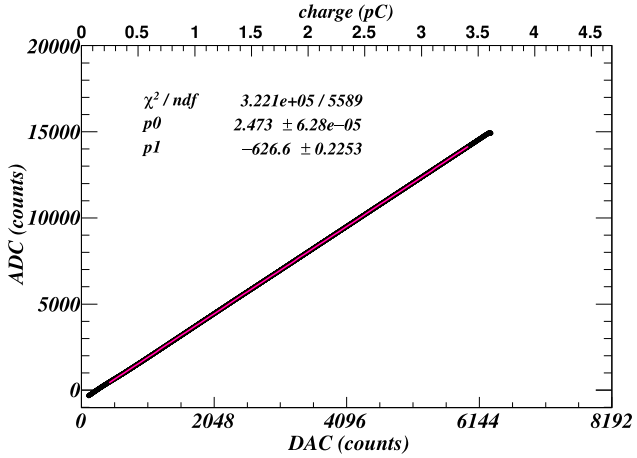

Fig. 8. ADC count versus DAC count for internal calibration measurements. The top axis shows the corresponding charge signal. A straight-line fit has been performed to the points.

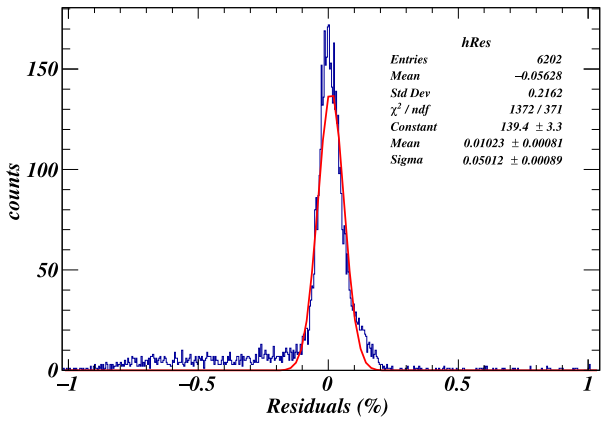

Fig. 9. Distribution of residuals with respect to a line fit performed to the calibration points in Fig. 8 in the 100–6300 DAC count interval. The residuals are normalized to the fit value.

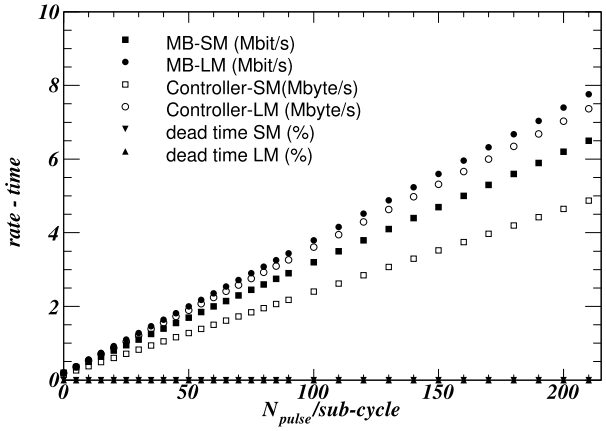

Fig. 10. Data rate for MBs and Controller versus N_{pulse} per cycle.

turned off to avoid the superimposing of physical signals to the calibration ones. The result of a linearity test performed on an MB electronics chain by using an on-board calibration mode is shown in Fig. 8. Each point represents the peak conversion (ADC counts) of a single ramp waveform versus the DAC counts set by the program. The baseline has been subtracted from the peak measurements. The corresponding charge values are reported on the top axis. By operating the DAC in a bipolar mode, the values in the range 0–8191 correspond to a positive voltage on the preamplifier, whereas the remaining range [8192–16 383] maps the negative values. In our configuration, only the positive pulse has been used. DAC values higher than 6300 saturate the ADC readout given the chosen operative range. A linear fit is performed on the measurement points in the DAC count interval (400–6000) and the distribution of percent difference is shown in Fig. 9. Except for a few DAC values below 400 counts, which exhibit a deviation from the fit line ranging between −1% and 1%, the residual distribution is well contained within 0.1%. Given the laser intensity variation (∼3%–5%) and the photosensor dependence with respect to the temperature (up to 10% for PMT) and bias voltage, this front-end design is able to operate in a wide dynamic range allowing the correction of shot-to-shot fluctuations at the per-mil level.

B. Data Acquisition Test

This section is devoted to the integration test of all the DAQ components at Fermi National Accelerator Laboratory (FNAL). The system under test in the final configuration consists of two crates containing six and eight fully functional MBs (connected to the photodetectors and front-end electronics), respectively, for the SM and LM, and a Controller for data readout. The laser control board distributes the BOF to the Controller chain and triggers the laser drivers according to the firing program. In fact, it has been programed to provide a subcycle rate of 100 Hz higher than the experiment's beam cycle (16 subcycles every 1.3 s).

In this setup, we have measured the data transfer rates by changing N_{pulse} per subcycle in a wide range of interest for the experiment. Fig. 10 shows linear behaviors both for MBs and Controllers. All the measurements have been performed by the Controller at the input of receivers (MB-SM and MB-LM) and at the output of the USB (Controller-SM and Controller-LM). Different transfer rates are due to different sizes between the SM and LM. The maximum value of MB data transfer is about 7.8 Mb/s obtained by the LM when the N_{pulse} value is 210, which corresponds to ∼7.4 Mbyte/s at the Controller exit, given the numbers of 8 MBs. To complete the DAQ characterization, we used the Controller monitoring facilities to track data transfers and processing activities in real time at the board level. In particular, the board is able to decouple

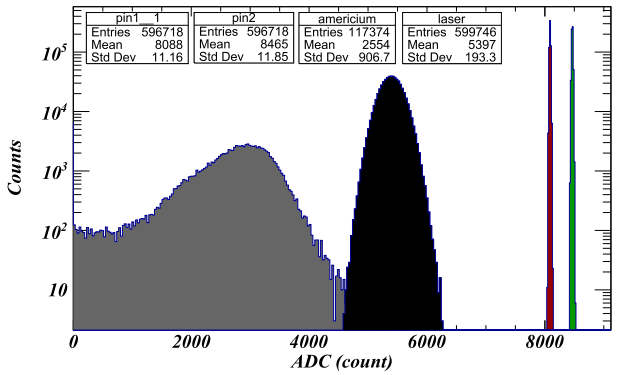

Fig. 11. Amplitude (ADC count) for the MB of SM #3. The PIN distributions (green and red) are much narrower than the PMT (black for laser pulses and gray for the Americium source). The discrimination between laser and Americium is implemented in hardware.

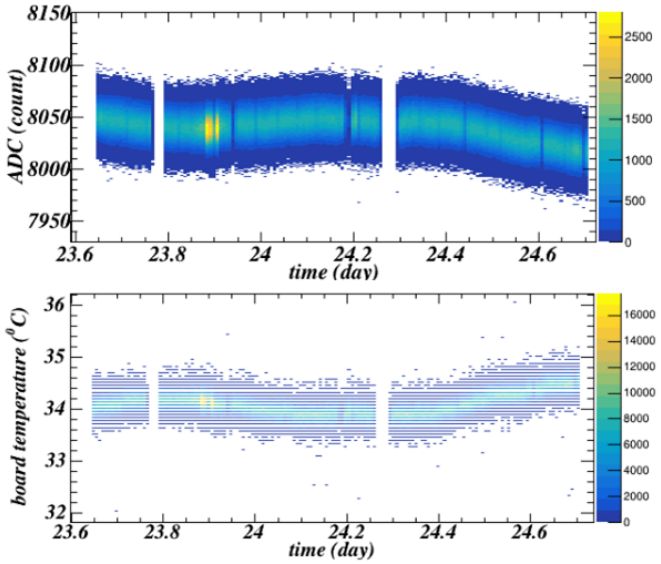

Fig. 12. PIN1 amplitude (top) and board temperature (bottom) of SM #3 monitored throughout one day of data taking.

the dead time components. It measures both the logical-OR of the busy signals of all the MBs housed in the crate and the Controller busy introduced when the internal USB FIFO Full-flag is asserted. Finally, the total dead time is the logical-OR of all dead time components, as shown in Fig. 10 for the SM and LM. The behaviors of data transfer rates and total dead time demonstrate that data frames shift smoothly from the MBs to the Controller USB device through several levels of buffer FIFOs in a broad range of pulse rates.

C. Monitoring Data

The last part of this section is devoted to the display of some monitoring information that is used to study the behavior of the calibration system data taking. Fig. 11 shows an example of ADC count distributions for the three channels of SM #3 (two PINs and 1 PMT). The entries correspond to about 3 h of data taking. Note the much larger distribution of the PMT amplitudes with respect to the PIN distributions. The behaviors of the ADC counts of PIN#1 and the board temperature are displayed in Fig. 12. Similarly, many other parameters can be monitored during the DAQ operation.

To conclude, these tests give us confidence that the system will be able to manage the photodetector operation and to handle the production run DAQ.

V. Conclusion

In this article, a custom DAQ system specifically designed to manage the photodetectors of Muon g-2 calibration has been described. The main elements are the front-end electronics board for signal processing, control and monitoring tasks, and the second level board that performs the complete data collection and implements the event-building at the crate level.

This article reports on several tests carried out on the MB to verify the readout chain and other functionalities such as the on-board calibration procedure, programmable by software, and slow control activity. All the DAQ components for the SM and LM have been successfully installed and integrated at Fermilab with the laser control board and the WFD readout. Studies on the data transfer rates and dead time have been performed under real conditions of data taking.

The possibility to control and acquire efficiently the photodetector signals of the calibration system within different operation modes facilitates the stability measurements and the study of the systematic effects in order to fulfill all the stringent requirements of the experiment.

The use of the Run Control allows easy management of the data taking and efficient monitoring both for front-end electronics and data processing (hardware and software components).

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