Single-phase power line conditioning with unity power factor under distorted utility voltage

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***Abstract*—The paper proposes a control method of a single-phase active power line conditioner (APLC) aimed at correcting the power factor of linear and non-linear loads supplied by distorted voltage utility. The method, that is based on the single-phase *p-q* theory and utilizes a third-order sinusoidal signal integrator, gets utility unity power factor and, at the same time, overcomes the shortcomings of the solutions pursuing utility sinusoidal current, namely the possible onset of un-damped resonance phenomena and the reduction in the energy delivery capabilities; moreover, the method makes the power factor correction robust against the supply distortion. The excellent performance of the method is substantiated by testing it by means of a hardware-in-the-loop setup.**

Keywords: **Single-phase Grid, Voltage Distortion, Unity Power Factor, Active Power Line Conditioners.**

I. INTRODUCTION

Compensation for the reactive power and/or abatement of the current harmonics produced by the loads are among the issues of major interest related to power quality [1]. Traditional solutions utilize capacitor banks and L-C filters. The modern solutions rely on Active Power Line Conditioners (APLCs) [2] since they exhibit better performance but, as an exchange, are more expensive. An answer to the cost concerns of APLCs consists in sharing their power electronics circuitry with other grid applications, such as connection of renewable energy sources to the grid [3]-[10] or implementation of "vehicle-to-grid" (V2G) services [11]-[13].

One of the most powerful and simple tools facing up the control of a three-phase APLC is the instantaneous power (or *p-q*) theory [15] and its subsequent modifications. Performance of the conventional compensation strategies based on the

p-q theory is degraded under non-ideal utility voltage conditions [16]. Solutions to such a degradation for three-phase APLCs are discussed in a number of papers [16]-[20]. In [16] modifications of the instantaneous power theory are compared for three conditions of non-ideal utility voltage and a more general compensation objective is set forth, obtaining balanced and sinusoidal source current in any condition of the supply voltage. In [17], where practical aspects of DSP implementation of the control system are addressed, a compensation approach based on the *p-q* theory concepts and pursuing unity power factor is proposed. In [18] self-tuning filters are deployed to improve the harmonic elimination executed by of an active power filter. In [19] a compensation algorithm is proposed which extracts the desired fundamental components of utility current and voltage for generating respectively the references of current magnitude and synchronization angle for APLC. In [20] a control algorithm built up around the third-order sinusoidal signal integrator (TOSSI) is proposed. However, the strategy behind the compensation solutions in [16], [18]-[20] is the achievement of a sinusoidal utility current, which leads to a number of shortcomings as it is discussed below in Section III.

The *p-q* theory, originally envisaged for three-phase power systems, was later revisited to be utilized for the single-phase systems [21] and applied to many cases. In [22], for example, it is utilized for the development of a phase-locked loop (PLL) appointed to detect phase and frequency of a single-phase utility voltage. In [23] it is utilized for the synthesis of the current reference for an APLC committed to the compensation for the reactive power and the filtering of the current harmonics absorbed by single-phase, distorting loads. In [24] and [4], a distorted utility voltage is examined and the single-phase *p-q* theory is utilized for the synthesis of the current reference for an APLC committed to the achievement of a sinusoidal utility current, which -as mentioned above- leads to a number of shortcomings. With the purpose of overcoming these shortcomings, this paper proposes a method that extends the unity power factor strategy to the APLC control [25] and presents an effective implementation of it. For simplicity, a single-phase APLC constituted by a dedicated apparatus and inserted in parallel to the load is considered. The synthesis of the current to be injected into the line connecting the utility to the load is obtained by a relatively simple control algorithm, which is a revisited version of the TOSSI-based approach presented in [20].

Organization of this paper is as follows. Section II describes the compensation of the reactive power carried out by APLCs for a single-phase sinusoidal utility. Section III deals with power line conditioning under utility voltage distortion; at first it explains the shortcomings of achieving a sinusoidal utility current and then expounds the rationale of the unity power factor strategy for single-phase APCLs. Section IV examines the advantages of such a strategy and describes an implementation of it enabling the accurate achievement of a unity power factor. Section V evaluates the impact of non-ideal low-pass filtering on the compensation performance. Section VI designs both the circuitry and the control system of an APLC taken as a study case. Section VII illustrates the setup of a prototypal APLC, implementing the proposed

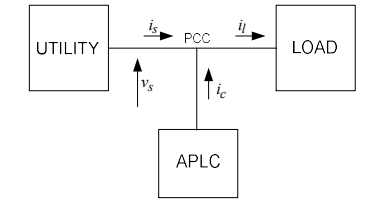
method and built up around a hardware-in-the-loop system; the Section, moreover, includes the results of tests that demonstrate the unity power factor correction capabilities of the setup. Section VIII exposes the paper conclusions.

II. SINGLE-PHASE APLC BASICS

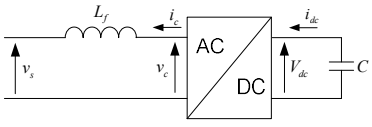
A. APLC scheme

Schematic of a single-phase utility with a load and an in-parallel APLC is drawn in Fig. 1 (a), where v_s and i_s are the grid voltage and the supply current, i_l is the current absorbed by the load, i_c is the current injected by the APLC into the line, and PCC is the Point of Common Coupling. For a linear R-L load, APCL is in charge of the task of compensating for the reactive power absorbed by the load; for a non-linear load, of filtering of the current harmonics absorbed by the load and, possibly, compensating for the reactive power. Therefore, current i_c must be tailored to the demanded compensating function. The circuital scheme of principle of an APLC is illustrated in Fig. 1 (b). It is comprising of a single-phase DC/AC voltage source converter (VSC), capacitor C in the converter DC side, and inductor L_f in the converter AC side. In Fig. 1 (b), v_c is the voltage across the AC terminals of the APLC, and V_{dc} and i_{dc} are the voltage and current in the DC side of the APLC, being voltage V_{dc} kept at a fixed value.

Block APLC in Fig. 1 (a) includes a control system that provides for synthesizing the reference of i_c, denoted with $i_{c,ref}$, for impressing i_c at the APLC output and for regulating V_{dc}.



(a)



(b)

Fig. 1. (a) Block scheme of single-phase system utility with load and APLC, (b) APLC circuital scheme.

B. Compensation current reference synthesis

The control potentialities of an APLC permit a fast synthesis of current $i_{c,ref}$ in accordance to the task demanded to the APLC. The synthesis is carried out by help of the *p-q* theory; for it to be used, two electrical quantities along orthogonal phases, commonly named α, β, must be at disposal. They are obtained from the single-phase quantities in Figs. 1 (a) and (b) as follows: quantities in the figures are directly associated to phase α, whilst quantities associated to fictitious phase β are suitably drawn out from those of phase α.

For a sinusoidal single-phase system, the quantities associated to phase β have the same magnitude and the phase shift of -π/2 with respect to the α quantities; for example [20], they can be calculated by processing the α quantities by

$$T_q(s) = \frac{k_1\omega_s^3}{s^3+k_2\omega_s s^2+(k_1+1)\omega_s^2 s+k_2\omega_s^3} \tag{1}$$

where ω_s is the utility angular frequency and k_1, k_2 are parameters to be selected in order to have the desired selectivity and the desired dynamic performance, respectively. Bode representation of (1) shows that it behaves as a low-pass filter and that, at ω_s, its magnitude is equal to 1 and its phase to -π/2.

As a matter of fact, current $i_{c,ref}$ is composed of two contributions, namely $i_{c,synt}$ and $i_{c,reg}$, as shown in Fig. 2. Current $i_{c,synt}$ compensates for the reactive power and the current harmonics absorbed by the load whilst the latter one replaces for the power losses in the APLC. Synthesis of $i_{c,synt}$ is executed by sequencing the following tasks:

i) sensing v_s and i_l,

ii) putting $v_{s\alpha}$ and $i_{l\alpha}$ equal to v_s and i_l,

iii) manipulating v_s and i_l through $T_q(s)$ to find out $v_{s\beta}$ and $i_{l\beta}$,

iv) calculating the instantaneous powers absorbed by the load by

$$\begin{aligned} p_l &= v_{s\alpha} i_{l\alpha} + v_{s\beta} i_{l\beta} = \bar{p}_l + \tilde{p}_l \\ q_l &= v_{s\beta} i_{l\alpha} - v_{s\alpha} i_{l\beta} = \bar{q}_l + \tilde{q}_l \end{aligned} \tag{2}$$

where p_l, q_l are the real and imaginary powers, and $\bar{p}_l$, $\bar{q}_l$ and $\tilde{p}_l$, $\tilde{q}_l$ are respectively the average and fluctuating parts of p_l, q_l, and

v) determining $i_{c,synt}$ by [15]

$$i_{c,synt} = \frac{v_{s\alpha} p_c + v_{s\beta} q_c}{v_{s\alpha}^2 + v_{s\beta}^2} \tag{3}$$

According to the direction of current i_c in Fig. 1, the reactive power compensation is achieved by setting $p_c = 0$ and $q_c = \bar{q}_l$, while harmonic filtering is achieved by setting $p_c = \tilde{p}_l$ and $q_c = \tilde{q}_l$ [15]. Note that the power terms p_l, q_l in (2)

include the contribution of fictitious quantities and therefore are two-times the real and imaginary powers absorbed by the load [14].

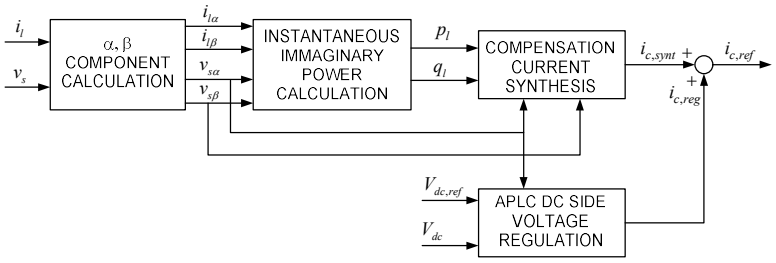


Fig. 2. Block scheme showing the synthesis of $i_{c,ref}$ under a sinusoidal utility voltage.

Current $i_{c,reg}$ plays the role of keeping charged at the constant value $V_{dc,ref}$ the voltage across the APLC DC side capacitor by offsetting for the power loss P_{loss} of the APLC circuitry. Magnitude of $i_{c,reg}$ is outputted by the closed-loop regulation of V_{dc}, whilst its phase is synchronized with the utility voltage.

Current $i_{c,ref}$ is then injected into the APLC AC side by a current control loop. Unity gain is assumed for the current loop so that, at steady-state, the actual values of $i_{c,synt}$ and $i_{c,reg}$ coincide with their references.

III. Injected APLC current reference synthesis under distorted utility voltage

The issue of getting the β component of v_s and i_l for a distorted voltage utility is somewhat intricate. As a matter of fact, using (1) gives rise to quantities $v_{s\beta}$ and $i_{l\beta}$ with different levels of distortion than $v_{s\alpha}$ and $i_{l\alpha}$ so that powers p_l, q_l calculated as in (2) are not useful for the synthesis of i_c by means of (3).

A. Sinusoidal utility current strategy

Paper [24] tackles the problem of synthesizing $i_{c,ref}$ by extracting the fundamental harmonic $v_{s\alpha,1}$ of $v_{s\alpha}$ and the corresponding (-π/2)-shift harmonic $v_{s\beta,1}$, and by using them to calculate the load instantaneous real power. An improved version of the solution presented in [24] has been developed in [4], and consists in delivering the α, β components of the utility voltages and load currents by processing v_s and i_l through the algorithm known as "second-order generalized integrator quadrature signal generator" [26].

The strategy behind papers [24] and [4] is to have a sinusoidal utility current. This strategy, however, leads to two serious inconveniences. One of them is the resultant power factor. Indeed, when a distorted utility voltage supplies a current sinusoidal and in-phase with $v_{s,1}$, the power factor is lower than one and the utility exhibits a reduced power capability. The other inconvenience is the possible onset of dangerous stress on the power system, as highlighted in [27].

To explicate this inconvenience, it comes useful the equivalent circuit of Fig. 3, where v_{sh} is the h-harmonic of v_s, L_s is the line inductance, C_r is the overall line capacitance -inclusive of the parasitic capacitance effects-, and R_l-L_l represents the load. The circuit describes the operation of a power system equipped with an APLC at the h-order harmonic of the utility voltage, and outlines that the parallel branch formed by APLC and load, hereafter termed as compensated load, behaves as an open circuit for the h-harmonic of current when a sinusoidal current i_l of angular frequency ω_s is absorbed by the branch. It follows that, on account of the un-damped resonance of the L_s-C_r circuitry, the h-harmonic v_{sh} of v_s produces an overcurrent in the mesh elements v_{sh}-L_s-C_r and an overvoltage across their terminals as soon as its angular frequency $h\omega_s$ is equal to $1/\sqrt{(L_sC_r)}$. Conversely, when current i_l is such as to get unity power factor of the compensated load, the latter one behaves as a resistance connected in parallel to C_r, and the occurrence of an un-damped resonance is prevented.

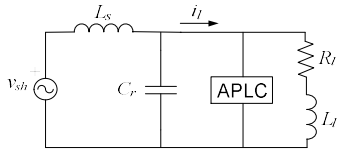


Fig. 3. Equivalent circuit of Fig. 1 (a) at the h-order harmonic of the utility voltage.

B. Unity power factor strategy

The strategy proposed in this paper pursues the goal of extending the achievement of a unity power factor to single-phase APLCs. The method used to implement the strategy starts by calculating the equivalent parallel resistance R_{eq_par} of the load. Let V_s be the utility voltage rms value and P is the active load power; it is

$$R_{eq\_par} = \frac{V_s^2}{P} \tag{4}$$

The instantaneous value of the utility current that yields a unity power factor could then be found by diving v_s by R_{eq_par}. However, determination of V_s and P would require the integration over one period of the respective time quantities, thus slowing down the dynamics of the compensation task. To circumvent this problem, the following procedure is conceived. At first, voltage and load current $v_{s\beta,1}$, $i_{l\beta,1}$ are calculated from v_s and i_l by processing v_s and i_l with the transfer function $T_q(s)$ in (1), whereas voltage and load current $v_{s\alpha,1}$ $i_{l\alpha,1}$ are calculated by processing v_s and i_l with the subsequent transfer function [20]:

$$T(s) = \frac{k_1\omega_s^2 s}{s^3+k_2\omega_s s^2+(k_1+1)\omega_s^2 s+k_2\omega_s^3} \tag{5}$$

Magnitude and phase of (5) at $\omega = \omega_s$ are equal to 1 and 0°, respectively, which means that (5) does not change the fundamental component of the processed quantities while it filters their harmonics. Under the hypothesis that $T(s)$ and $T_q(s)$ operate as an ideal low-pass filter, the instantaneous real power drawn by the load, calculated from $v_{s\alpha,1}$, $v_{s\beta,1}$, $i_{l\alpha,1}$ and $i_{l\beta,1}$, is expressed as

$$p_{l,1} = v_{s\alpha,1} i_{l\alpha,1} + v_{s\beta,1} i_{l\beta,1} \tag{6}$$

At steady-state, $p_{l,1}$ is constant and, in accordance to [14], is designated as the fundamental active power absorbed by the load. It yields to an equivalent parallel load resistance given by

$$R_{t,par} = \frac{v_{s\alpha,1}^2 + v_{s\beta,1}^2}{p_{l,1}} \tag{7}$$

Then, current reference $i_{c,synt}$ is synthesized as

$$i_{c,synt} = i_l - \frac{v_s}{R_{t,par}} \tag{8}$$

Processing of the quantities according to the proposed method is represented in Fig. 4.

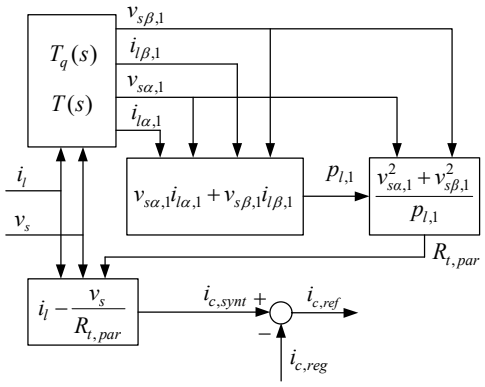


Fig. 4. Proposed method block diagram representation.

It can be demonstrated that, for an R-L load, $R_{t,par}$ is lower than R_{eq_par}. Then, the active power drawn by the compensated load and, consequently, the active power that the utility delivers after compensation is higher than the needed one. The in-excess power P_{exc} would enter into the APLC and would produce an increase of V_{dc} beyond its reference, if V_{dc} were not regulated. The closed-loop regulation of V_{dc} avoids this inconvenience by decreasing $i_{c,reg}$ and, with it, the active power delivered by the utility so as to proper balance the active power between compensated load and utility.

After compensation, the utility provides the following current:

$$i_{s,comp} = i_l - i_{c,synt} + i_{c,reg} = \frac{v_s}{R_{eq\_par}} \tag{9}$$

By (9), the utility apparent power S and active power P are

$$S = V_s I_{s,comp} = \frac{V_s^2}{R_{eq\_par}} \tag{10}$$

$$P = \frac{1}{T}\int_0^T v_s i_{s,comp} dt = \frac{V_s^2}{R_{eq\_par}} \tag{11}$$

where T is the utility period, and $I_{s,comp}$ is the rms value of $i_{s,comp}$. Equations (10) and (11) point out that S is equal to P, meaning that, thanks to the proposed method, the utility has a unitary power factor.

IV. STRATEGY COMPARISON

It can be easily proved that in the single-phase system with a sinusoidal utility voltage the sinusoidal utility current strategy and that one of unity power factor lead to the same results. Hence, it is of interest to examine and compare their features under distorted utility voltage.

Let the utility voltage be formulated as

$$v_s = V_{1M}\cos(\omega_s t) + \sum_{h=2}^{\infty} V_{hM}\cos(h\omega_s t - \theta_h) \tag{12}$$

where subscript M stands for peak magnitude. The load current is

$$i_l = I_{1M}\cos(\omega_s t - \varphi_1) + \sum_{h=2}^{\infty} I_{hM}\cos(h\omega_s t - \theta_h - \varphi_h) \tag{13}$$

The active power absorbed by the load is

$$P = \frac{1}{T}\int_0^T v_s i_l dt = V_{s,1} I_{s,1}\cos\varphi_1 + \sum_{h=2}^{\infty} V_{s,h} I_{s,h}\cos\varphi_h \tag{14}$$

where $V_{s,1} = V_{1M}/\sqrt{2}$, $I_{s,1} = I_{1M}/\sqrt{2}$, $V_{s,h} = V_{hM}/\sqrt{2}$ and $I_{s,h} = I_{hM}/\sqrt{2}$.

A. Sinusoidal utility current strategy

By this strategy the utility current after compensation is

$$i_{s,comp} = \sqrt{2}\frac{P}{V_{s,1}}\cos(\omega_s t) \tag{15}$$

The apparent power delivered by the utility after compensation is

$$S = V_s I_{s,comp} = P\sqrt{1 + \sum_{h=2}^{\infty}\left(\frac{V_{s,h}}{V_{s,1}}\right)^2} \tag{16}$$

By (16), the power factor of the compensated load is

$$PF = \frac{1}{\sqrt{1 + \sum_{h=2}^{\infty}\left(\frac{V_{s,h}}{V_{s,1}}\right)^2}} = \frac{V_{s,1}}{V_s} \tag{17}$$

Eq. (17) shows that the sinusoidal current strategy yields a power factor lower than one.

B. Unity power factor strategy

By this strategy, the utility current after compensation is

$$i_{s,comp} = \frac{v_s}{R_{eq\_par}} = \frac{\sqrt{2}P}{V_{s,1}\left[1+\sum_{h=2}^{\infty}\left(\frac{V_{s,h}}{V_{s,1}}\right)^2\right]}\left[\cos(\omega_s t) + \sum_{h=2}^{\infty}\frac{V_{s,h}}{V_{s,1}}\cos(h\omega_s t - \theta_h)\right] \tag{18}$$

The apparent power delivered by the utility after compensation is

$$S = V_s I_{s,comp} = P \tag{19}$$

Eq. (19) underlines that $S = P$, thus confirming what demonstrated by (10) and (11), i.e. the effective achievement of a unitary supply power factor. Consequently, for a certain distortion of the supply voltage, the utility current has a rms value lower than the sinusoidal supply current approach. This can be readily verified by comparing the rms value of the currents in (18) with (15).

V. NON-IDEAL FILTERING IMPACT

The proposed method described in Subsection III.B has been worked out under the hypothesis that the low-pass filtering eliminates the harmonics of the involved quantities. Since this is a simplifying hypothesis, it is useful to investigate the effect of the non-ideal low-pass filtering executed by (1) and (5) on the compensation effectiveness.

Let v_s and i_l, as given respectively in (12) and (13), be filtered by $T(s)$ and $T_q(s)$. By setting $s = jh\omega_s$, it is

$$\begin{aligned} v_{s\alpha} &= V_{1M}\cos(\omega_s t) + \sum_{h=2}^{\infty} k_h V_{hM}\cos(h\omega_s t - \theta_h - \delta_h) \\ v_{s\beta} &= V_{1M}\sin(\omega_s t) + \sum_{h=2}^{\infty} \frac{k_h}{h} V_{hM}\cos(h\omega_s t - \theta_h - \gamma_h) \end{aligned} \tag{20}$$

$$\begin{aligned} i_{l\alpha} &= I_{1M}\cos(\omega_s t - \varphi_1) + \sum_{h=2}^{\infty} k_h I_{hM}\cos(h\omega_s t - \theta_h - \varphi_h - \delta_h) \\ i_{l\beta} &= I_{1M}\sin(\omega_s t - \varphi_1) + \sum_{h=2}^{\infty} \frac{k_h}{h} I_{hM}\cos(h\omega_s t - \theta_h - \varphi_h - \gamma_h) \end{aligned} \tag{21}$$

where

$$k_h = |T(jh\omega_s)| = \frac{1}{\sqrt{\left(1+\frac{1-h^2}{k_1}\right)^2 + \frac{k_2^2}{h^2 k_1^2}(1-h^2)^2}} \tag{22}$$

$$\delta_h = Arg[T(jh\omega_s)] = -\pi + \tan^{-1}\left[\frac{k_2(1-h^2)}{h(k_1+1-h^2)}\right] \tag{23}$$

$$\gamma_h = Arg\left[T_q(jh\omega_n)\right] = \pi - \tan^{-1}\left[\frac{h(k_1+1-h^2)}{k_2(1-h^2)}\right] \tag{24}$$

As equations (20) and (21) show, harmonic attenuation produced by $T(s)$ is lower than that produced by $T_q(s)$. To make the two filtering actions as much similar as possible, $T(s)$ can be replaced by the following transfer function:

$$TD(s) = \frac{k_1\omega_s^2 s}{s^3+k_2\omega_s s^2+(k_1+1)\omega_s^2 s+k_2\omega_s^3} \cdot \frac{2\zeta\omega_s s}{s^2+2\zeta\omega_s s+\omega_s^2} \tag{25}$$

Attenuation of harmonics produced by (25) and (1) is the same, on condition that

$$\zeta = \frac{1}{2}\sqrt{1-\frac{1}{h^2}} \tag{26}$$

Eq. (26) gives a different value of ζ for each harmonic of order h. However, for $h \geq 2$, the range of variation is limited, since it is $0.433 \leq \zeta < 0.5$. Low-order harmonics are the most difficult to be filtered. Fortunately, the supply voltage is not frequently affected by a second harmonic; on the contrary, it is often affected by a third harmonic. Therefore, a convenient choice is to set $h = 3$ in (26), obtaining $\zeta = 0.47$. However, for frequencies over 50 Hz, magnitudes of (1) and (26) almost coincides also for f ≠ 150 Hz as illustrated by the Bode diagrams in Fig. 5.

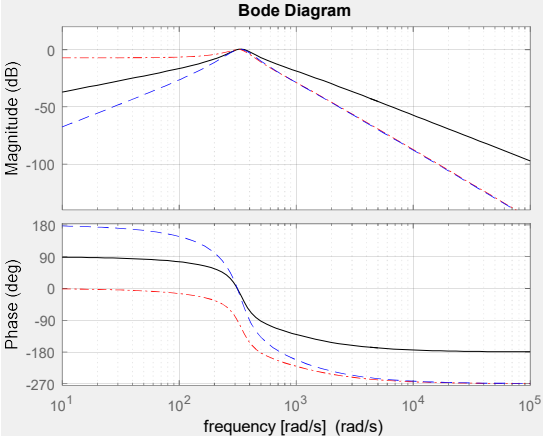


Fig. 5. Bode diagrams of $T_q(s)$ (red dash-dotted curves), $TD(s)$ (blue dashed curves) and $T(s)$ (black solid curves) for $k_1 = 1.4$, $k_2 = 3.18$ [20] and $\zeta = 0.47$.

An issue to be considered is that the frequency of the fundamental component of the utility voltage does not always coincide with 50 Hz. In fact, the standard EN 50160 tolerates that, for interconnected power systems, the utility voltage frequency is 50 Hz ± 1% for 99.5% of time in a year. As a consequence, it is necessary to guarantee good performance of the compensation for the frequency varying at least in the range 49.5 Hz – 50.5 Hz. This requires a suitable choice of parameters k_1 and k_2 of the transfer functions (1) and (25). The lower is k_1 the higher is the selectivity and the bandwidth

of the filter, thus increasing its harmonic mitigation as well as its ability to track the variations of the input signal. However, too high selectivity reduces the robustness of the system to variations of the line frequency. Moreover, increasing of the filter dynamics beyond a certain level leads to a low-damped behavior. In the same way as for k_1, the lower is k_2 the higher are the filter dynamics but, opposed to what happens for k_1, the lower is the selectivity of the filter. A good compromise between the different performance requirements is found in [20], were k_1 and k_2 are set equal respectively to 1.4 and 3.18.

Bode diagrams of the transfer functions (25) and (1) in the frequency range 49.5 Hz – 50.5 Hz are plotted in Fig. 6. The diagrams shows that, when the frequency slightly deviates from 50 Hz, the magnitude and the phase of the fundamental component of the utility voltage change less than 2% and 5°, respectively.

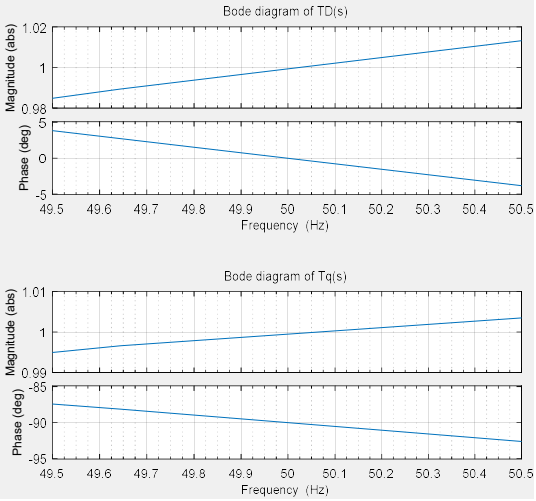


Fig. 6. Bode diagrams of $TD(s)$ and $T_q(s)$ in the frequency range 49.5 Hz – 50.5 Hz.

VI. APLC DESIGN AND PERFORMANCE ASSESSMENT

A single-phase APLC has been designed for reactive power compensation and harmonic filtering of a load composed of a linear R,L branch and an in-parallel, non-linear branch formed by a diode rectifier with a DC-link capacitive filter. To test the performance of the APLC in harsh conditions, it has been assumed that the load is supplied by a highly distorted utility voltage containing - in addition to the fundamental component of 220V - harmonics of 3, 5 and 7-th order with

magnitudes of 10% of 220 V for the third harmonic and of 5% of 220 V for both fifth and seventh harmonics. The line resistance is 0.03Ω and its inductance is 0.1mH.

The APLC is built up around a single-phase IGBT bridge. On account of the load power and its power factor, the designed nominal current of the IGBT bridge is 7A rms. The DC-link voltage V_{dc} is set equal to 400V. Such a relatively high value is due to the distorted utility voltage and highly distorted current to be filtered and meets the need for the APLC to be able to deliver the required current even in the worst conditions.

The inductor L_f in Fig. 1 (b) is sized in order that each high-order current harmonic caused by the PWM control of the APLC does not exceed 5% of the APLC nominal current I_{cN}. Considering that, among the harmonics of v_c ensuing from a unipolar PWM control, that one of low order with the highest magnitude is at twice the PWM frequency, the inductance of L_f is calculated by the following formula:

$$L_f = \frac{V_{c\_sw}}{2\omega h_{sw} I_{c\_sw}} \tag{27}$$

where subscript sw stands for switching frequency. In (27), ω is the angular frequency of the fundamental component, h_{sw} is the harmonic order at the switching frequency, and V_{c_sw} and I_{c_sw} are the rms values of the voltage and current harmonics at the switching frequency. The value of V_{c_sw} depends on the modulation index. However, in the calculation of L_f, it was set at 220 V because, in the worst cases, its value is close to the fundamental component of V_c.

Capacitor C (Fig. 1b) is sized bearing in mind that the main contribution to the ripple of V_{dc} is given by the power fluctuations at twice the mains frequency. Setting the steady-state value of the DC voltage ripple $\Delta V_{dc\%}$ at 1%, the capacitance of C is calculated by the following formula:

$$C = \frac{V_{cN} I_{cN}}{\omega V_{dc}^2 \Delta V_{dc\%}} \tag{28}$$

where V_{cN} and I_{cN} are the rms nominal voltage and current values at the APLC output. Equation (28) is commonly used to size the dc-bus capacitor for photovoltaic inverters and PWM rectifiers operating at single-phase unity power factor [28]. Nevertheless, the equation is applicable also to single-phase grid connected converters delivering reactive power since, by perusing [28], it is obtained for any value of the displacement angle between the fundamental components of AC side current and voltage.

The block schemes respectively of the AC side current control and the DC side voltage regulation, as implemented in the APLC control system, are detailed in Figs. 7 and 8. Harmonic filtering requires a very fast current control able to track the reference current as precisely as possible. In order to fulfill such a requirement, an improved deadbeat control with current-tracking error compensation (CTEC) for three-phase APLCs was proposed in [29]. While the deadbeat control in [29] is not suited to a single-phase APLC, the CTEC algorithm is applicable and is used here to supplement the PI current

controller in the intervals where the APLC reference current derivative is higher than a preset threshold level. Moreover, as suggested in [30], the phase margin of the current control loop is enhanced by including a predictive compensation of the digital control period delay (PCDCPD) in the current feedback.

Regulation of the voltage across the APLC DC side capacitor must ensure the balance of the active power flow from the utility to the compensated load. Specifications for the regulation system are zero steady-state error and somewhat low bandwidth, here set at 1 Hz, since the active power balance does not call for high dynamics. However, this bandwidth has to be much lower than the frequency of the active power fluctuations (twice the mains frequency) to impede that the ripple of V_{dc} alters the reference current $i_{c,reg}$.

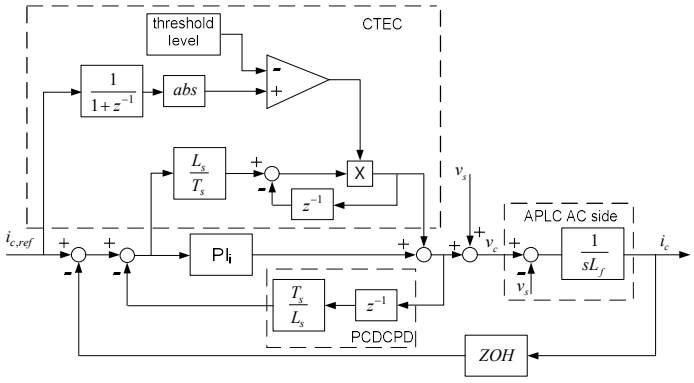


Fig. 7. Block scheme of APLC current i_c control with current-tracking error compensation (CTEC) and predictive compensation of the digital control period delay (PCDCPD).

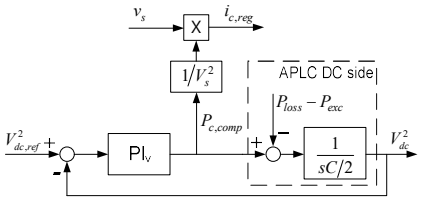


Fig. 8. Block scheme of APLC DC-bus voltage V_{dc} regulation.

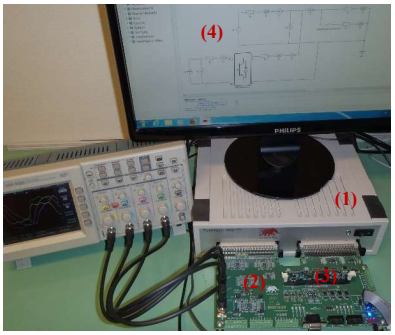
Data of the APLC and control system parameters obtained by applying the aforementioned design criteria are reported in Table I.

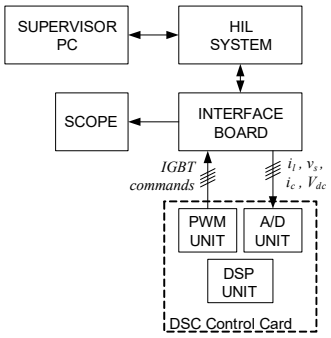
TABLE I. APLC and control system data

Parameters in (1) and (25)	k_1	1.4	Damping factor ζ in (25)		0.47
	k_2	3.18			
DC bus			AC output terminals		
Capacitor C		4 mF	Inductor L_f		3 mH
voltage control closed-loop bandwidth		1 Hz	current control closed-loop bandwidth		2 kHz
PI_v controller parameters	k_p	$5*10^{-5}$	PI_i controller parameters	k_p	$7*10^{-2}$
	τ_i	1 s		τ_i	2 ms
DC side voltage reference		400 V	Switching frequency		20 kHz

VII. APLC CONTROL SYSTEM TEST

The APLC control system developed with the proposed method to pursue the unity power factor strategy was set up by uploading the control algorithm written in C programming language on a TMS320F28335-based DSP control card [29]. The control system was then tested by means of the hardware-in-the-loop (HIL) facility shown in Fig. 9 (a), constituted by a Typhoon HIL400 emulator [32] and an HIL400 Docking Station hosting TI DIM100 DSP Cards [33], playing the Docking station the role of interface board between the TMS320F28335-based DSP control card and the Typhoon HIL400 emulator. The hardware-in-the-loop facility is described by the block diagram of Fig. 9 (b), were the emulator (HIL system), programmed and controlled by a supervising PC, replicates the power system, the loads and the hardware section of the APLC (DC/AC power converter, DC bus capacitor, output filtering inductor) and delivers signals proportional to the load current i_l, the utility voltage v_s, the APLC current i_c and the APLC dc-link voltage V_{dc} at its output. The output signals of the emulator are sent to the DSP control card via the interface board. For its part, the DSP unit processes the received signals, previously digitized by the A/D unit, and, by help of a PWM unit, produces the IGBT commands that are sent to the emulator via the interface board. The code of the control algorithm loaded in the DSP unit is described by the block diagrams in Figs. 4, 7 and 8.





a) b)

Fig. 9. Hardware-in-the-loop facility: a) picture showing 1) Typhoon HIL400 emulator, 2) HIL400 Docking Station for TI DIM100 DSP Cards, 3) TMS320F28335 control card, 4) graphical interface of the development software Typhoon HIL Control Center; b) block diagram.

VSC of the APLC and the associated circuitry were modeled by the graphical interface of the development software Typhoon HIL Control Center. The APLC losses are emulated in the Typhoon HIL model by putting a resistance of 30mΩ in the APCL DC side to account for the conduction losses in the VSC devices, and a resistance of 10mΩ in the APCL AC side to account for the parasitic losses in the filter inductor. Typhoon HIL Control Center does allow modeling of the switching losses in the VSC devices that, therefore, are neglected. This does not affect the significance of the results since i) they are a small fraction of the power drawn by the compensated load, and ii) the overall APLC efficiency exceeds 95%. Moreover, the APLC model has been also simplified by ignoring switching delays, sensor errors and finite bandwidth.

The Typhoon HIL400 emulator is endowed with an I/O digital connector and an I/O analog connector. Analog outputs are signals in the range ±5V, equal to the measured quantities divided by the scaling factor that is 10 for currents and 100 for voltages.

The APLC control system was submitted to a number of tests, in both steady-state and transient conditions. The linear branch of the load draws a power of 1.3 kVA whilst the non-linear branch draws a power of 0.9 kVA, values that are in the range of the typical single-phase loads. In the first test, the reactive power compensation abilities of the APLC are proven by operating the linear branch of the load at steady state and disconnecting the non-linear branch. The results of the test, traced in Fig. 10, show that the behavior of the compensated load is like that of a resistance since the waveform

of the current i_s replicates that one of the utility voltage v_s. Table II reports the power factor and the magnitude of the load and utility current harmonics. The data in the table outline that the harmonics of the compensated current increase with respect to the load current. This trend is correlated to the magnitudes of the utility voltage harmonics and to the APLC operation, which removes the filtering action of the load inductance by compensating for it. The results of the test are fully compliant with the goal of the unity power factor strategy and substantiates its achievement. The data obtained for different values of the supply frequency reveal that the APLC performance is insensitive to slight deviations of the frequency from its nominal value.

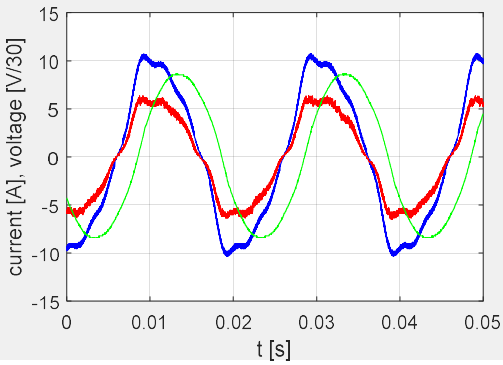


Fig. 10. Reactive power compensation test: scaled supply voltage v_s (blue trace), load current i_l (green trace), line current i_s (red trace).

TABLE II. Linear load: current harmonics as a percentage of the fundamental component of the load current for different values of supply frequency.

Frequency		49 Hz		50 Hz		51 Hz	
Current		Load	Supply	Load	Supply	Load	Supply
	PF	0.679	0.998	0.672	0.997	0.664	0.997
Harmonics [%]	1st	100	69.7	100	68.9	100	68.0
	3rd	4.4	6.2	4.4	5.3	4.3	5.5
	5th	1.4	4.1	1.4	3.9	1.4	3.8
	7th	1.1	4.2	1.1	4.2	1.0	4.2
	9th	< 0.5	0.5	< 0.5	0.6	< 0.5	0.6
	11th	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5
	13th	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5

	15^{th}	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5
	17^{th}	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5
	19^{th}	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5

In the second test, the current filtering abilities of the APLC are proven. The non-linear branch is operated at steady state and the linear branch is disconnected. The results of the test, traced in Fig. 11, show that - similarly to the linear branch - the behavior of the compensated load is like that of a resistance and this is a further demonstration of the proper functioning of the control system. Table III reports the power factor and the magnitudes of the non-linear load and supply current harmonics. The data in the table outline that the harmonics of the compensated current are strongly reduced with respect to the load current. Nevertheless, residual harmonics of order 3, 5 and 7 with some magnitude are present. They are produced by the supply voltage harmonics applied to the compensated load of resistive type. Again, the results of the test are fully compliant with the goal of the unity power factor strategy and substantiates its achievement. Moreover, here too the APLC performance is insensitive to slight deviations of the frequency from its nominal value.

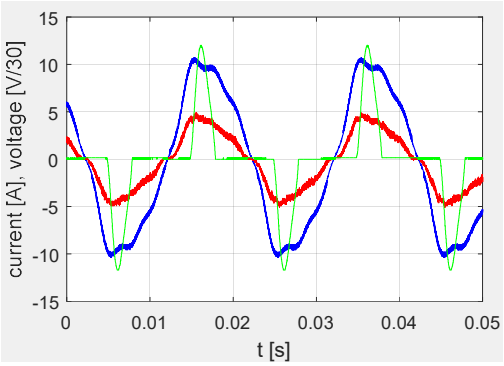


Fig. 11. Harmonic filtering test: scaled supply voltage v_s (blue trace), load current i_l (green trace), line current i_s (red trace).

TABLE III. Non-linear load: current harmonics as a percentage of the fundamental component of the load current for different values of supply frequency.							
Frequency		49 Hz		50 Hz		51 Hz	
Current		Load	Supply	Load	Supply	Load	Supply
	PF	0.660	0.992	0.664	0.992	0.668	0.991
Har	1^{st}	100	99.2	100	99.1	100	99.1

	3rd	85.2	13.6	84.9	14.0	84.5	14.3
	5th	60.6	8.1	59.8	7.8	58.8	7.6
	7th	34.1	5.1	32.9	5.1	31.7	5.0
	9th	13.8	1.4	12.9	1.3	12.1	1.3
	11th	7.3	< 0.5	7.6	0.5	7.9	0.5
	13th	7.6	< 0.5	7.8	0.5	7.9	0.5
	15th	4.6	0.9	4.4	0.9	4.2	0.9
	17th	< 0.5	0.7	< 0.5	0.8	< 0.5	0.8
	19th	2.2	< 0.5	2.4	< 0.5	2.5	< 0.5

In a third test, the abilities of the APLC to compensate simultaneously for a linear and non-linear load are proven. Both the linear branch and the non-linear branch of the load are operating at steady state. The results of the test are traced in Fig. 12. Both the waveforms reported in Fig. 12 and the value of the compensated power factor, which is less than one of a nothing also in case of slight deviations of the supply frequency (see Table IV), demonstrate once again that the APLC performance is excellent also when it carries out two different compensating actions and, at the same time, is robust against a frequency deviation. Table IV reports the power factor and the magnitudes of the load and supply current harmonics. As in the previous case, the data of the table outline that the harmonics of the compensated current are highly reduced with respect to the load current, but residual harmonics of order 3, 5 and 7 with some magnitude are present because of the resistive behavior of the compensated load under distorted utility voltage.

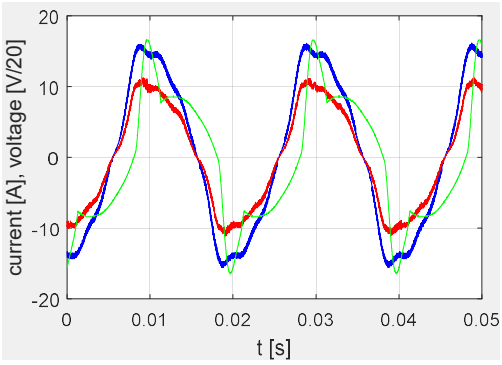


Fig. 12. Test of simultaneous reactive power compensation and harmonic filtering: scaled supply voltage v_s (blue trace), load current i_l (green trace), line current i_s (red trace).

TABLE IV. Linear and non-linear load: current harmonics as a percentage of the fundamental component of the load current for different values of supply frequency.

Frequency		49 Hz		50 Hz		51 Hz	
Current		Load	Supply	Load	Supply	Load	Supply
	PF	0.803	0.999	0.800	0.999	0.798	0.999
Harmonics [%]	1st	100	89.1	100	88.9	100	88.8
	3rd	33.4	9.6	33.5	9.0	33.6	9.1
	5th	22.3	5.3	22.1	5.2	22.0	5.0
	7th	12.0	4.1	11.7	4.2	11.4	4.2
	9th	4.9	< 0.5	4.6	< 0.5	4.4	0.5
	11th	2.6	< 0.5	2.7	< 0.5	2.8	< 0.5
	13th	2.7	< 0.5	2.8	< 0.5	2.8	0.5
	15th	1.6	0.6	1.6	0.7	1.5	0.6
	17th	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5
	19th	0.8	< 0.5	0.9	< 0.5	0.9	< 0.5

In the last test, dynamic performance of the APLC is checked. At first, the linear load branch is brought to operate at steady state. Subsequently, at t = 0.02 s in Fig. 13, the non-linear load branch is suddenly connected. The traces of the ensuing transients show that the APLC current reacts immediately and settle to the required value in less than two supply periods. The transient results close the testing activities on the APLC control system, validating its setup and the method developed for its design.

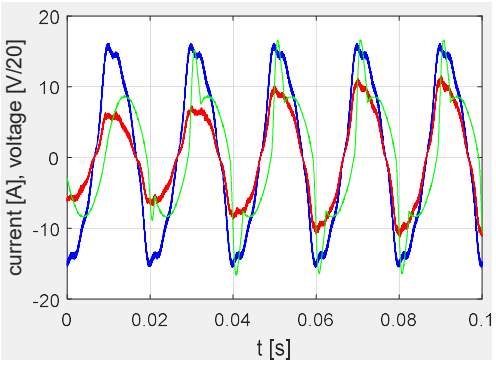


Fig. 13. Response to the connection of the non-linear load: scaled supply voltage v_s (blue trace), load current i_l (green trace), line current i_s (red trace).

VIII. CONCLUSIONS

The paper has dealt with the compensation of single-phase linear and non-linear loads under distorted utility voltage by means of an APLC. The strategy of achieving unity power factor for the utility, which has never applied before to single-phase systems, has been examined and validated by arranging and testing a control system setup for APLC. Unlike the existing strategy of compensating the single-phase loads to get a sinusoidal utility current, the unity power factor strategy has the merits of avoiding the possible occurrence of an un-damped resonance in the power system and increasing the power delivery of the utility. A method intended to get a unity power factor has been proposed and developed by exploiting the *p-q* theory potentialities. Implementation of the method has taken some steps, namely derivation of the α component and the fictitious β component of the quantities involved in the APLC control, sizing of the passive components of the APLC circuitry, arrangement of the control loops of both APLC output AC current and input DC voltage with formulation of their specifications, and design of the loop controllers. A theoretical analysis and tests carried out by means of a hardware-in-the-loop equipment have demonstrated the effectiveness of both method and its implementation.

The research activity presented in the paper is planned to continue with the implementation of an experimental single-phase vehicle-to-grid (V2G) apparatus, which will enable to carry out a full experimental validation of the proposed method and to test the performance of an APLC integrated in a V2G system.

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