


A Novel Thyristor-Based CSI Topology With Multilevel Current Waveform for Improved Drive Performance

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Abstract—Load-commutated inverters (LCIs), combined with wound-field synchronous machines (WFSMs), can be an excellent solution for high power drives, but their present technology suffers from important drawbacks related to low power factor, large torque pulsations, and poor starting performance. This paper presents a new LCI design intended to overcome the mentioned limitations. An SCR-based forced-commutation circuit is added to the common inverter topology to obtain a five-level waveform for the stator current. This leads to significantly reduced current harmonics and torque pulsations, in addition to bringing benefits in terms of lower additional losses. As a further advantage, the proposed design allows for a significant power factor enhancement. Finally, it enables the WFSM to be started with a much smoother torque compared to the traditional pulsed operating mode of conventional LCI drives. Simulation studies are conducted on a high-power drive scheme to show the aforementioned improvements. Also, a reduced-scale laboratory prototype of a WFSM drive system is tested to verify the feasibility of the proposed converter.

Index Terms—Current harmonics, five-level current source, forced commutation, load-commutated inverter (LCI)-fed drive, power factor improvement, start up, torque pulsations.

I. INTRODUCTION

CURRENT-SOURCE inverters (CSIs) are still widely used in synchronous machine drives especially for medium-voltage high-power industrial and ship propulsion applications [1], [2] thanks to some key advantages they offer with respect to their voltage-source counterpart. Inherent short-circuit protection and regenerative capability, simpler structure, lower voltage stresses over the machine insulations and the semiconductor devices and the suppression of travelling wave phenomena when the motor is fed via long cables are among these advantages [3], [4]. Similar to voltage-source inverters (VSIs), pulse

width modulation (PWM) techniques can be utilized in CSIs which employ self-turn-OFF power electronic switches such as Gate Turn-Off Thyristors (GTOs) and Insulated Gate Bipolar Transistors (IGBTs) in order to eliminate the low-ordered harmonic contents of the machine stator current [3]–[6]. In CSI-fed machine drives, however, forced commutation of the dc-link current creates voltage spikes due to motor phase inductances. In order to absorb the voltage spikes, a three-phase capacitor bank is installed at the CSI output which can also play the role of a filter for high-frequency current harmonics produced by the PWM switching [7]–[9]. A rule of thumb in designing the capacitor bank is that the lowest frequency of the stator current harmonic components must be far away from the resonance frequency of the circuits created by the capacitor bank and the machine magnetizing and leakage inductances [10]. Consequently, the capacitance needed will normally vary between 0.3 and 0.5 p.u. of the machine base impedance for switching frequencies of approximately 400 Hz [3].

On the other hand, high frequency switching of the power devices is not desirable in some high-power applications, with power ratings typically over 10 MW [11]–[13], since it decreases the converter efficiency. On the contrary, in load-commutated inverter (LCI)-fed wound-field synchronous motor (WFSM) drives, the efficient, reliable, and inexpensive thyristor (SCR) devices are naturally commutated at the machine operating frequency when the machine is working in the over-exciting mode. This load commutation results in high converter efficiency which can be higher than 99% when the drive operates under the rated conditions [3]. Furthermore, the need for bulky capacitor bank is removed in this drive.

All this said, it is a matter of fact that today's LCI technology suffers from some well-known weaknesses, such as large line-side and motor-side current harmonics, low power factor and efficiency of the WFSM, poor start-up performance, and large torque pulsations [3]. The line-side current harmonics can be effectively reduced to acceptable levels by adopting a 12-pulse or 24-pulse configuration for the line-side converter [14], [15]. Instead, no effective solutions are presently available in LCI drive state-of-the-art to cope with the other issues that relate to motor operation. As regards the power factor, in fact, a safe motor-side converter operation with no commutation failure risk requires a firing angle usually not higher than 150°, which implies power factor values below 0.9.

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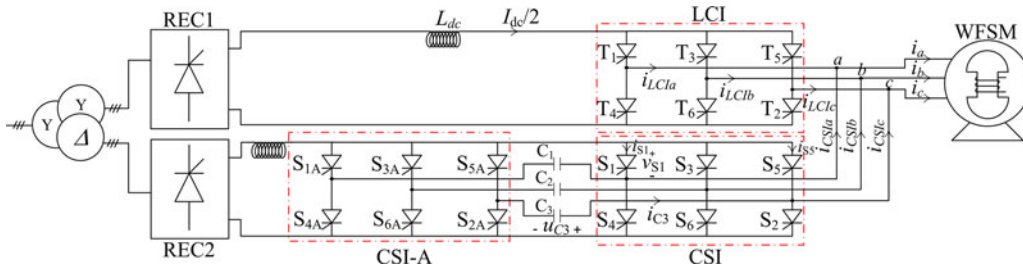


Fig. 1. Proposed five-level-current-source topology.

Regarding start-up, it is known that at low speeds (usually under 10% of rated) motor counter electro-motive forces are insufficient for SCR load commutation and a so-called pulsed operating mode is employed in the industry [16], [17]; this gives rise to high torque ripples that may result in severe shaft-line mechanical resonance issues [18].

Finally, in regards to torque pulsations during normal (load-commutated) operating mode, the use of dual three-phase WFSMs can bring benefits thanks to the disappearance of the main torque harmonic component (sixth order) [19]; however, the solution is not always feasible, e.g., it does not fit the cases when LCIs are used to supply grid-connected (three-phase) generators for start-up before synchronization or in pumped storage hydropower plants [20].

The combination of VSI-based active filter and the SCR-based LCI has been proposed in the literature for the high-power induction and synchronous machine drives [7]–[9], [13], [21]–[24]. These research works mainly pursue three objectives which are

- 1) the removal of output capacitor bank in PWM-CSI;
- 2) natural commutation of the SCRs as the main switches;
- 3) improving the above-mentioned drawbacks of the LCI-fed machine drives.

For instance in [24], the machine could be started from standstill via the VSI keeping the LCI OFF, while at normal operating speeds the VSI acts as an active filter attenuating the stator current harmonics and reducing the torque pulsations. However, in high-voltage applications, a multilevel configuration is needed for the VSI to reduce the voltage stresses over the switches. Also, a series inductance must be connected at the VSI output acting as a controlled current source in addition to a capacitor bank to absorb the harmonics arising from the PWM switching. This LC filter could draw the resonance current from the VSI. Therefore, an active damping control scheme should be used to damp the LC resonance. Most importantly, the hybrid VSI–CSI topology tends to reduce the advantage of converters based on SCRs only. In addition, the VSI-related problems in high-voltage drives such as short-circuit protection still remain.

In this paper, a novel five-level-CSI (FLCSI) topology is presented to significantly enhance LCI drive operation in the following respects: reduction of torque harmonics in a three-phase LCI-fed WFSM; increase in WFSM power factor; strong reduction of start-up torque pulsations; reduction of motor current harmonics; and related additional losses. These advantages are obtained through the addition of suitable SCR- and capacitor-based circuits, so as to change motor currents from

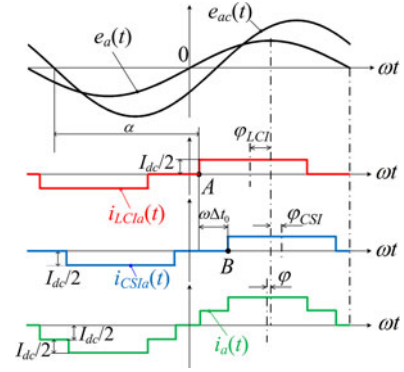


Fig. 2. Phase a voltages and currents of LCI and CSI.

their usual quasi-square shape into a five-level waveform and to reduce current fundamental shift angle with respect to motor voltage (with consequent power factor increase).

The effectiveness of the proposed new concept is illustrated and positively assessed through accurate numerical simulations of a high-power WFSM drive system and through experimental implementation of a low-power prototype.

II. PROPOSED FIVE-LEVEL-CURRENT-SOURCE CONFIGURATION CONCEPT

The proposed FLCSI structure is shown in Fig. 1. It consists of a usual LCI combined with a thyristor-based CSI, which is, in turn, split into a couple of SCR bridges, called CSI and CSI-A (A standing for auxiliary). Neglecting the dc-link current ripple, the output currents of both converters, i.e., i_{LCIa} and i_{CSIa} , taking phase a as an example, feature the usual quasi-square waveform and are identical except for a phase displacement $\omega\Delta t_0$, as shown in Fig. 2 (the line-side converters are controlled to output the same dc-link current $I_{dc}/2$). In the figure, the motor phase a voltage $e_a(t)$ and line-to-line voltage $e_{ac}(t)$ neglecting commutation notches (so focusing the attention on the fundamentals) are considered.

The resultant waveform of $i_a(t) = i_{LCIa}(t) + i_{CSIa}(t)$ will have five levels, i.e., $0, \pm I_{dc}/2$, and $\pm I_{dc}$ (see Fig. 2). In particular, if the phase displacement between i_{LCIa} and i_{CSIa} is set equal to 30° , the amplitude of the fifth and seventh order current harmonics becomes 5.36% and 3.83% of the fundamental, respectively, while they would be 20% and 14.35% if the usual LCI topology with quasi square-wave currents were employed. The 30° displacement is selected so as to minimize the current total harmonic distortion (THD) as illustrated in Fig. 3.

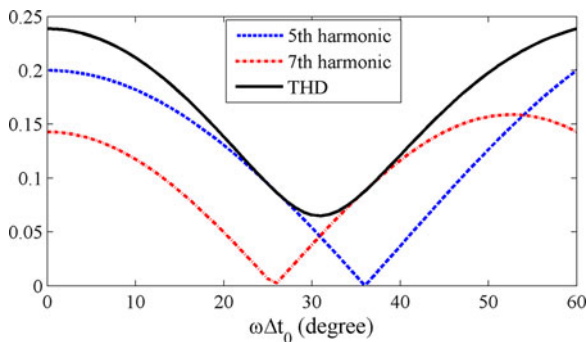


Fig. 3. Fifth and seventh harmonic amplitudes (relative to fundamental) and THD (considering 5th and 7th components only) for the current i_a as a function of $\omega\Delta t_0$ in the proposed converter structure.

Out of the three thyristor bridges included in the proposed topology, the converter indicated as LCI in Fig. 1 operates as a usual load-commutated inverter. To guarantee safe commutations, it must be operated with a suitable firing angle α (adequately lower than 180°), as illustrated in Fig. 2, where thyristor T_1 is shown to turn ON at point A. Conversely, CSI thyristors are force commutated as it will be explained in Section III, with no risk of commutation loss; therefore, they can be safely fired with a 30-electrical-degrees delay with respect to LCI thyristors (for instance S_1 is fired at point B, which is placed $\omega\Delta t_0 = 30$ electrical degrees after A). Assuming $t = 0$ as the zero-crossing instant of the phase voltage e_a , from Fig. 2 it can be inferred that instant t_B is given by

$$t_B = (-\pi + \pi/6 + \alpha + \pi/6)/\omega = (\alpha - 2\pi/3)/\omega \quad (1)$$

being $(-\pi + \pi/6)/\omega$ the negative derivative zero crossing of e_{ac} , that is the reference instant for firing T_1 .

As a result, not only a better current harmonic spectrum is obtained (as mentioned above), but also a power factor enhancement occurs. In fact, Fig. 2 shows that the fundamental components of $i_{LCI}(t)$ and $i_{CSI}(t)$ have, respectively, a leading (φ_{LCI}) and lagging (φ_{CSI}) phase shift with respect to $e_a(t)$. Consequently, the phase shift (φ) of the fundamental component of the total current $i_a(t)$ will be reduced compared to φ_{LCI} .

In addition to reducing the current distortion and increasing the power factor, the forced-commutation circuit composed of CSI and CSI-A can be used, at standstill or low speeds, as a high-performance starter, too, achieving a definitely better torque than with the usual pulsed operating mode of normal LCIs [25]. This will be discussed in more detail in Section IV.

III. FORCED-COMMUTATION CIRCUIT PRINCIPLES OF OPERATION

So far, several forced-commutation circuits have been proposed in the literature to turn-OFF the thyristors in high power CSI-fed induction motor drives. One of the first forced commutation schemes was proposed in [26] and utilized, for instance, in [27] and [28]. The commutation circuit is composed of one capacitor (with one terminal connected to the machine neutral point) and two auxiliary thyristors and operates only during ma-

chine starting. In this circuit, depending upon the commutation period length, pulse width of stator current is less than 120° . Moreover, at very low speeds, when the electromotive force (EMF) cannot charge the capacitor enough to ensure the commutation, the technique of delayed gating is employed, which needs a voltage sensor. One other drawback of this circuit is the reduction of electromagnetic torque to half during commutation periods since the auxiliary thyristor currents are of zero sequence and do not take part in torque production. Besides, the neutral point of the machine should be accessible. Autosequential current-fed inverters are another example of these circuits [16], [29], which are composed of six additional ac capacitors and six diodes. However, the latter are in series with the main switches, so they have to be selected with the same current rating as the SCRs and cause significant extra losses; moreover they suffer from large machine spike voltages during commutations [16]. A VSI in parallel with the main CSI can also commutate the SCRs [22], but this leads to lose the advantage of converters based on SCRs only.

In this paper, a different external forced-commutation circuit is proposed. It consists of six auxiliary thyristors $S_{1A} - S_{6A}$ and three ac capacitors $C_1 - C_3$, of equal capacitance C (see Fig. 1). This solution can be already found in the literature as a part of CSI-fed induction motor drives [29]. In addition to being a low cost and efficient circuit due to the inexpensive SCR switches, the current rating of the auxiliary thyristors is much less than that of the main devices since the dc-link current flows through $S_{1A} - S_{6A}$ only during commutation transients.

In this section, details are given on how forced commutation is obtained in the CSI bridge using the auxiliary converter CSI-A. The description includes mathematical details (see Section III-A) which are however required to obtain some practical dimensioning rules regarding capacitors C_1 , C_2 , and C_3 as well as auxiliary thyristors $S_{1A} - S_{6A}$ (see Sections III-B–III-D).

A. Forced Commutation Dynamic Analysis

In order to investigate the forced commutation of converters CSI and CSI-A, the WFSM is modeled as a series connection of a phase EMF—e.g., $e_a(t) = \sqrt{2}E \sin(\omega t)$, taking phase a as an example—and a commutation inductance L_C [30], being ω the electrical angular frequency. As a case study, let us consider the forced commutation process where S_1 turns ON and S_5 turns OFF, which occurs at instant B (see Fig. 2). Before such instant, T_1 , T_6 , S_5 , and S_6 are conducting and C_3 is charged with voltage u_{C3} , having amplitude $+U_{C0}$ according to the polarity shown in Fig. 1. The current and voltage waveforms over a period of the electrical quantities $T = 2\pi/\omega$ are shown in Fig. 4 for thyristors S_1 , S_5 , and capacitor C_3 , along with a zoomed view of the commutation process between S_1 and S_5 .

In order to turn S_5 OFF and S_1 ON, S_{5A} is fired (together with S_1) at an instant t_B corresponding to point B in Fig. 2. As a result, the voltage U_{C0} insisting on capacitor C_3 is applied across S_5 and turns it OFF. This turn-OFF process is abrupt (practically instantaneous) because there is no inductance slowing the decay of the current in S_5 . Consequently, the current i_{CSIc} , which is

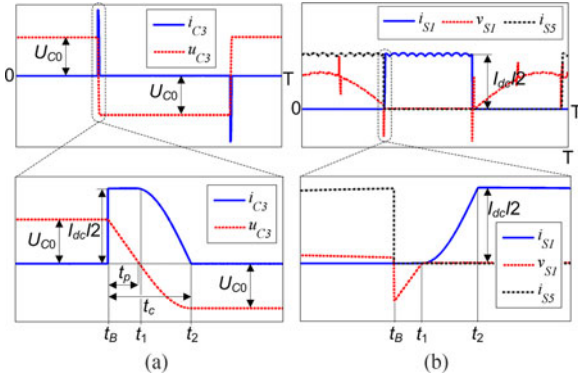


Fig. 4. (a) Voltage and current of capacitor C_3 in one period (top) and its zoomed view for commutation between S_5 and S_1 (bottom); (b) i_{S1} , v_{S1} , and i_{S5} in one period (top) and its zoomed view during commutation (bottom).

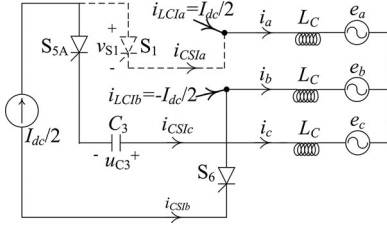


Fig. 5. Equivalent circuit for $t_B < t < t_2$.

equal to $I_{dc}/2$, is forced to flow through the series of S_{5A} and C_3 . This causes capacitor voltage u_{C3} to linearly decay according to the following equation:

$$u_{C3} = U_{C0} - [I_{dc}/(2C)] (t - t_B). \quad (2)$$

From (2), by setting u_{C3} to zero, the time interval t_p during which a reverse voltage is applied to the outgoing thyristor S_5 (see Fig. 4) is obtained as

$$t_p = 2CU_{C0}/I_{dc}. \quad (3)$$

The value of t_p must be larger than the thyristor turn-OFF time t_q , the condition for S_5 turn-OFF being $t_{p-\min} \geq t_q$.

With reference to Fig. 4, the further instants t_1 and t_2 are identified. Between t_B and t_1 , S_1 is not conducting (being reversely polarized) and a constant current $I_{dc}/2$ flows through C_3 and S_{5A} . At $t = t_1$, a direct voltage is applied to S_1 causing it to start conducting together with S_{5A} . Finally, at $t = t_2$ the commutation completes with all the current $I_{dc}/2$ transferred from S_{5A} to S_1 causing S_{5A} to turn OFF. The overall transient between t_B and t_2 is governed by the equivalent circuit shown in Fig. 5 and, hence, by the following differential equation:

$$\begin{aligned} v_{S1}(t) + u_{C3}(t) - L_c di_c(t)/dt - e_c(t) \\ + e_a(t) + L_c di_a(t)/dt = 0 \end{aligned} \quad (4)$$

where $e_a(t) - e_c(t) = e_{ac}(t) = \sqrt{6}E \sin(\omega t - \pi/6)$ is the line-to-line voltage that drives the commutation transient.

For $t_B \leq t \leq t_1$, $i_a(t) = i_{LC1a}(t) = I_{dc}/2$ and $i_c(t) = i_{CS1c}(t) = I_{dc}/2$ [see Figs. 4(a) and 5]. Hence, $di_c(t)/dt$ and $di_a(t)/dt$ in (4) are equal to zero for $t_B \leq t \leq t_1$. Therefore, by setting $v_{S1}(t)$ equal to zero in (4) for $t = t_1$ and replacing

$u_{C3}(t_1)$ from (2) into (4), t_1 is obtained from the following equation:

$$U_{C0} - [I_{dc}/(2C)] (t_1 - t_B) = -\sqrt{6}E \sin(\omega t_1 - \pi/6). \quad (5)$$

For $t_1 < t < t_2$, S_1 begins conducting together with S_{5A} [see Fig. 4(b)], which causes i_{CS1a} to increase and i_{CS1c} to decrease. At $t = t_2$, currents i_{CS1a} and i_{CS1c} reach $I_{dc}/2$ and zero, respectively, and consequently S_{5A} turns OFF and the commutation is completed. Hence for $t_1 < t < t_2$

$$i_{CS1a} + i_{CS1c} = I_{dc}/2, \quad i_{CS1a} = i_a - I_{dc}/2, \quad i_{CS1c} = i_c. \quad (6)$$

Since $i_{CS1c} = -C du_{C3}/dt$ (see Fig. 5), extracting u_{C3} from (4), deriving it, and using (6), the following equation is obtained for $t_1 < t < t_2$ [v_{S1} is zero in (4) neglecting its ON-state voltage drop]:

$$2LCd^2 i_{CS1a}/dt^2 + i_{CS1a} = I_{dc}/2 + Cd(e_c - e_a)/dt. \quad (7)$$

If the transfer of current from phase a to phase c is assumed to be much faster than the variation rate of phase EMFs, that is

$$t_2 - t_B \ll 2\pi/\omega. \quad (8)$$

$e_{ac}(t)$ in (7) can be regarded as constant and equal to its value at $t = t_1$, or

$$e_{ac}(t) \cong \sqrt{6}E \sin(\omega t_1 - \pi/6). \quad (9)$$

Thus, (7) can be simply solved imposing $i_{CS1a} = di_{CS1a}/dt = 0$ at $t = t_1$ as initial condition. Defining $\omega' = 1/\sqrt{2LC}$, for $t_1 < t < t_2$ the following solution is found:

$$i_{CS1a} = (I_{dc}/2) \{1 - \cos[\omega'(t - t_1)]\}. \quad (10)$$

$u_{C3}(t)$ for $t_1 < t < t_2$ can be found from (4), (6), (9), and (10) as

$$u_{C3}(t) \cong -\sqrt{6}E \sin(\omega t_1 - \pi/6) - LC\omega' I_{dc} \sin \omega'(t - t_1). \quad (11)$$

Finally, at $t = t_2$, $i_{CS1a} = I_{dc}/2$ and (10) gives

$$t_2 - t_1 = \pi/(2\omega'). \quad (12)$$

At $t = t_2$, a period of commutation is finished and for reasons of symmetry u_{C3} reaches $-U_{C0}$ (see Fig. 4) in order to ensure the turn-OFF of S_2 by firing S_{2A} at $t = t_B + T/2$. Hence, from (11) and (12) we have

$$\begin{aligned} U_{C0} = -u_{C3}(t_2) \cong \sqrt{6}E \sin(\omega t_1 - \pi/6) \\ + (I_{dc}/2)\sqrt{2LC/C}. \end{aligned} \quad (13)$$

The same process occurs at $t_B + T/6 < t < t_2 + T/6$, when S_6 is turned OFF by firing S_{6A} .

B. Capacitor Dimensioning Considerations

The voltage U_{C0} given by (13) depends on the operating point and in particular varies with α . Using (1) for t_B and assuming $t_B \cong t_1$ we get

$$U_{C0} \cong \sqrt{6}E \sin(\alpha - 5\pi/6) + (I_{dc}/2)\sqrt{2LC/C} \quad (14)$$

which shows that U_{C0} decreases as α decreases (assuming that firing angles larger than 150° are not allowed). So the minimum

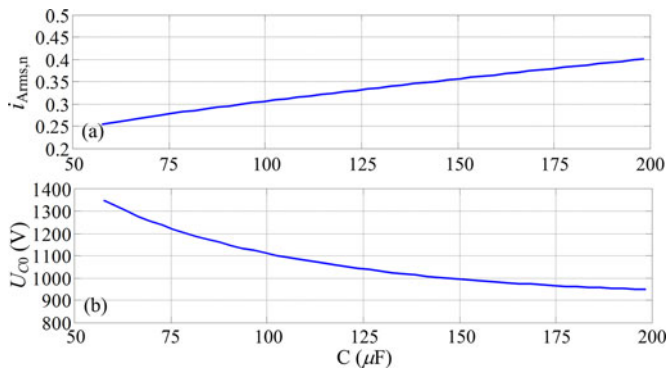


Fig. 6. (a) RMS value of the auxiliary thyristor current normalized to that of the main thyristors and (b) the capacitor voltage as a function of capacitance for rated motor operation.

value of U_{C0} occurs when the LCI is operating at its minimum firing angle α_{\min} . However, the minimum value of U_{C0} can be also obtained from (3) in the limit case where $t_p = t_q$. Now, if we equate the minimum U_{C0} obtained in this way to that given by (14) with $\alpha = \alpha_{\min}$, the following algebraic relationship results:

$$t_q = t_p \cong (2\sqrt{6}EC / I_{dc}) \sin(\alpha_{\min} - 5\pi/6) + \sqrt{2CL_C}. \quad (15)$$

From (15), it is possible to find the minimum capacitance C_{\min} required to ensure safe commutation as a function of parameters α_{\min} , t_q , L_C , and E .

As an example, if $\alpha_{\min} = 150^\circ$ from (15) we get

$$C_{\min} = t_q^2 / (2L_C). \quad (16)$$

For illustration purposes, let us assume the drive data given in Appendix A, with an SCR turn-OFF time of $100 \mu\text{s}$ and L_C approximately equal to $0.5 (L'_d + L'_q) = 87 \mu\text{H}$ [30] (being L'_d and L'_q the machine subtransient inductances along rotor d and q axes). In this case, C_{\min} can be computed to be of $57 \mu\text{F}$ according to (16).

C. Auxiliary SCR Dimensioning Considerations

As explained above, the auxiliary thyristors ($S_{1A} - S_{6A}$) only conduct during the commutation intervals. For example, using (10) the current through S_{5A} over one period T is

$$i_{S_{5A}} = \begin{cases} I_{dc}/2 & t_B < t < t_1 \\ I_{dc}/2 - i_{CS1a} = (I_{dc}/2) \cos[\omega'(t - t_1)] & t_1 < t < t_2 \\ 0 & t_2 < t < t_B + T \end{cases} \quad (17)$$

and its rms value is

$$i_{S_{5A}rms} = (I_{dc}/2) \sqrt{((t_1 + t_2)/2 - t_B)/T} \quad (18)$$

where t_B , t_1 , and t_2 in the above-mentioned equation are obtained according to (1), (5), and (12), respectively. The maximum value of the auxiliary-SCR rated current, normalized to that of the main thyristors ($i_{A_{rms,n}}$) of the LCI and CSI bridges (see Fig. 1), is plotted in Fig. 6(a) as a function of the capac-

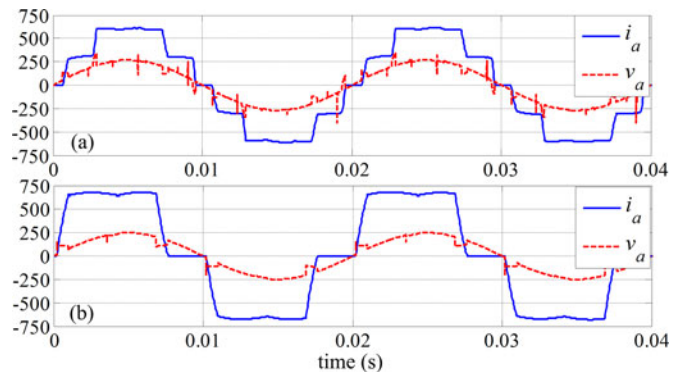


Fig. 7. Phase a voltage and current of the machine at the frequency of 50 Hz: (a) FLCSI and (b) LCI.

TABLE I
HARMONICS OF THE PHASE CURRENT RELATIVE TO ITS FUNDAMENTAL PEAK VALUE

	$i_{a1,max}$ (A)	i_{a5} (%)	i_{a7} (%)	i_{a11} (%)	i_{a13} (%)	THD (%)
Five-level CSI	447	0.7	7.2	8.2	4.2	13.06
Conventional LCI	517	19.4	11.7	6.3	4.5	24.12

itance for the rated operating condition, i.e., rated speed and torque of the machine specified in Appendix A. From the figure, the maximum value of the auxiliary thyristor current rating is 40% for a capacitance of $200 \mu\text{F}$.

D. General Dimensioning Considerations

As regards the sizing of capacitors C_1 , C_2 , C_3 , their voltage U_{C0} using (14) is plotted in Fig. 6(b) as a function of capacitance for rated conditions. To sum up, we can conclude that an increase in the capacitance C causes an increase in the current rating of the auxiliary thyristors, while it decreases the peak capacitor voltage U_{C0} . Thus, a trade off should be made to have reasonable values for capacitor voltage rating together with an acceptable current capability for auxiliary thyristors (see Section III-C).

IV. SIMULATION RESULTS

The proposed FLCSI is simulated applying it to the supply of the WFSM described in Appendix A. The field-oriented control strategy proposed in [31] is implemented to control the speed. In order to limit the capacitor voltage on one side and the current rating of the auxiliary thyristors on the other, a capacitance of $150 \mu\text{F}$ is selected. Fig. 7 illustrates the phase voltage and current of the machine when it is driven by a conventional LCI and the proposed FLCSI, at the speed of 1500 r/min and with the same load torque. It can be seen that the displacement angle of the fundamental current component with respect to the voltage is nearly zero for the proposed topology (meaning almost unity power factor operation) and 23° for the conventional LCI design (see Section II).

The amplitude of the phase current harmonic components relative to the fundamental i_{1max} is shown in Table I for the FLCSI and the conventional LCI. It can be seen from Table I

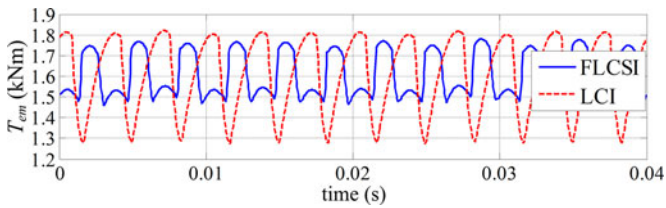


Fig. 8. Electromagnetic torque of the motor at the frequency of 50 Hz.

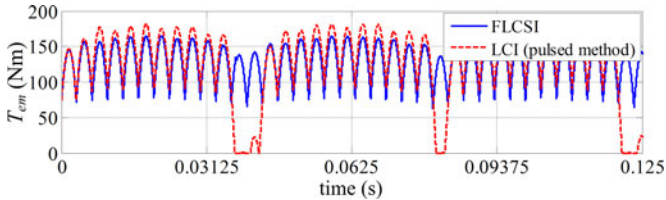


Fig. 9. Electromagnetic torque during start up (4 Hz operation).

that the power factor improvement yields lower dc-link current for a given equal torque ($I_{dc}/2$ is around 300 A for the FLCSI while I_{dc} is around 670 A for the LCI). As a further beneficial effect, also the field current (and hence field losses) decreases (from 138 to 123 A) in the new topology thanks to the better power factor.

Torque pulsations are also decreased considerably as shown in Fig. 8, where the amplitude of 6th and 12th harmonics of the motor electro-magnetic torque T_{em} are, respectively, 8% and 4% of the average torque for the FLCSI and 15% and 5% for the conventional LCI. The average torque is equal to 1602 Nm for both cases.

Finally, as previously mentioned, the machine can be started via the forced-commutation circuit (CSI and CSI-A), omitting to release the firing pulses for LCI thyristors. In Fig. 9, the machine electromagnetic torque waveforms at starting are shown for both the proposed scheme and the known pulsed method at the speed of 0.04 p.u. As it can be seen, the torque notches of the pulsed method are removed in the proposed scheme.

V. EXPERIMENTAL RESULTS

The proposed multilevel current source inverter is experimentally implemented to assess its capability in controlling three-phase WFSM. A picture of the laboratory prototype is shown in Fig. 10. Thyristors of the type SKKT 57/22 E are employed as the main switches (in rectifiers, LCI and CSI) and BT152-800R thyristors for the auxiliary circuit (CSI-A). The control algorithm described in [31] is implemented on dspIC30F4011 microprocessors.

In Fig. 11, the switching pattern for the main thyristors in CSI and the auxiliary thyristors in CSI-A is shown. Considering the fact that the switching of the thyristors is carried out according to the rotor position, the pulses distinguished in blue are released to the CSI-A thyristors during normal and starting operation. The red pulses in Fig. 11 are provided to appropriately charge the capacitors at starting from standstill to guarantee the forced-commutation approach. For instance, assume that at standstill

capacitors C_1 , C_2 , C_3 are discharged, i.e., $U_{C0} = 0$. At $\theta = \theta_0$ thyristors S_1 and S_6 are fired and start conducting. According to Fig. 11, at this instant S_{3A} is also fired to charge C_2 to $-U_{C0}$ (see Fig. 1). Therefore, at the next commutation instant, i.e., at $\theta = \theta_0 + \pi/3$, S_6 can be turned OFF by firing S_{6A} . S_{4A} is also fired at $\theta = \theta_0 + \pi/3$ in addition to S_2 to charge C_1 enough to make it ready to apply the negative voltage across S_1 by firing S_{1A} at $\theta = \theta_0 + 2\pi/3$. After starting the machine, the red pulses can be removed.

As shown in Fig. 10(b), a WFSM coupled to a separately-excited dc generator is used in the experiments. Ratings and parameters of the synchronous motor are reported in Appendix B. According to these parameters, the subtransient inductance is equal to 19.5 mH. Furthermore, the turn-OFF time t_q of the main thyristors in CSI is equal to 80 μ s. Consequently, (16) shows that a minimum capacitance of 0.16 μ F is needed to guarantee the safe commutation. However, a capacitance [see Fig. 10(a)] equals to 2 μ F is employed in order to reduce U_{C0} at full-load operating condition, because, as it will be explained later, it impacts the voltage ratings of the auxiliary thyristors.

In Fig. 12, the stator voltage and current waveforms are shown for the starting operation (frequency of 2 Hz or rotor speed of 40 r/min). As it can be seen from this figure, the stator voltage is not adequate to guarantee a good commutation (with no commutation failures) in the LCI, especially when the starting torque is high or, in other words, the starting current is high. Therefore, the stator current is supplied by the CSI circuit and there is no need to implement the conventional dc-link pulsing method.

Subsequently, experimental results are compared at normal operating conditions for two cases: 1) the WFSM is supplied by the FLCSI and 2) the WFSM is supplied by the conventional LCI. The rotor speed is 450 r/min and the load is the same in the two cases. In the second case, the firing angle is set to 150° (higher firing angles result in commutation failure); therefore, the fundamental power factor angle is 30° (leading). On the other hand, setting $\alpha = 150^\circ$ for the LCI in the first case (even if a slightly higher values of α would be allowed because the commutating current is halved) results in a fundamental power factor angle of 15° (leading). This yields to lower dc-link current ($I_{dc}/2 = 2.8$ A) of the proposed configuration compared to the traditional LCI case ($I_{dc} = 6.1$ A).

The average value of the field current is 1.8 A with the FLCSI topology, while in the case in which the WFSM is driven by the LCI it is 2.1 A. This proves a certain advantage of the proposed FLCSI configuration also in terms of lower field current and consequently lower field losses compared to the case of conventional LCI-fed drives.

The stator phase voltage and current waveforms for the first case (the WFSM is supplied by the FLCSI) are shown in Fig. 13. From Fig. 13(b), a firing angle of about 150° is observable for the LCI. Thus, the fundamental component of i_{LCIa} leads the stator phase voltage by $\varphi_{LCI} = 30^\circ$. On the other hand, the firing angle for CSI switches is 180°, which leads to zero displacement angle between the fundamental component of i_{CSIa} and the phase voltage (φ_{CSI} in Fig. 13(c)). As a result, the fundamental power factor angle, i.e., φ in Fig. 13(d) is 15° (leading).

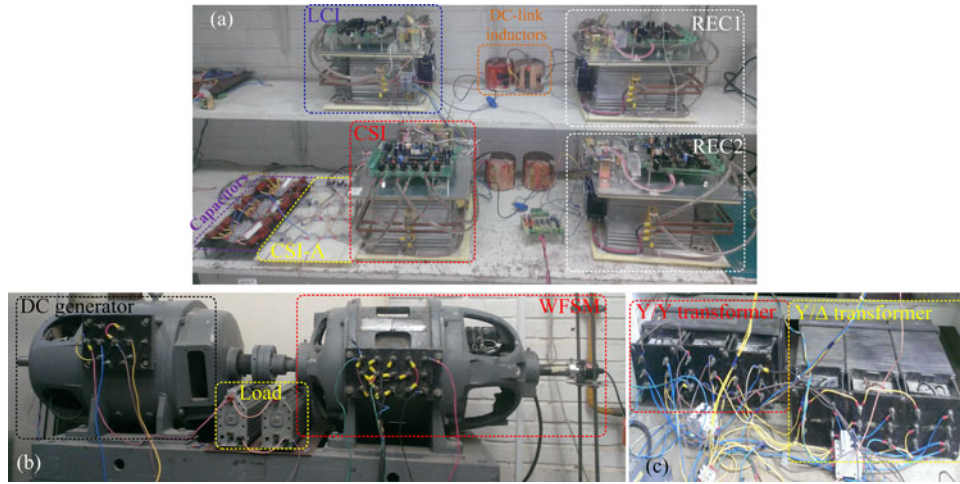


Fig. 10. Experimental set-up of the proposed FLCSI, (a) converters shown in Fig. 1, (b) WFSM used as the motor and dc generator used as the load, (c) input transformers.

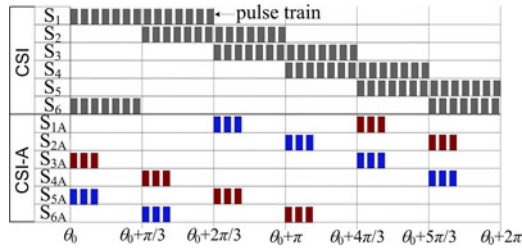


Fig. 11. Switching pattern of the CSI and CSI-A switches (red pulses have to be released only at starting).

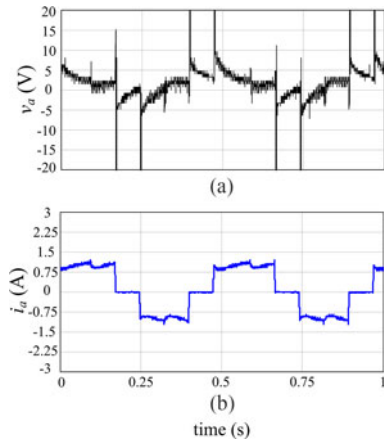


Fig. 12. Experimental waveforms for the (a) stator voltage and (b) stator current at the speed of 40 r/min or frequency of 2 Hz (the LCI circuit is not working).

In Fig. 14, the harmonic spectrum of the quasi-square wave LCI current shown in Fig. 13(b) is compared to that of the five-level waveform shown in Fig. 13(d). Results show that the THD is remarkably reduced in a five-level current (11.5%) with respect to the conventional three-level current waveform (26%). Also, the amplitude of the fifth and seventh components of the stator current is reduced significantly (respectively for

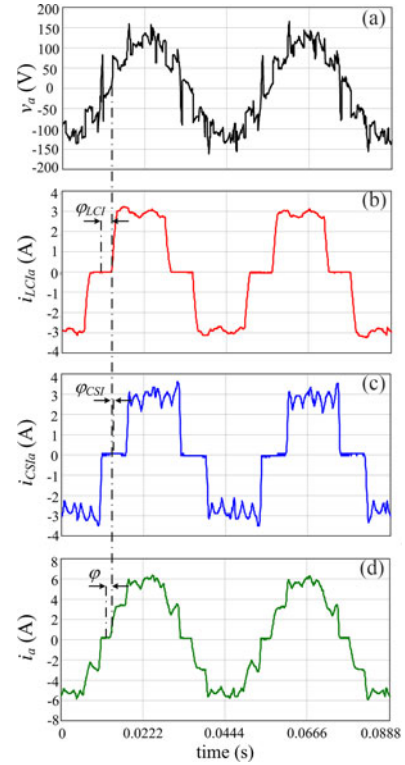


Fig. 13. Experimental waveforms for the normal operation of the proposed FLCSI at the speed of 450 r/min, (a) stator phase voltage, (b) LCI output current, (c) CSI output current, and (d) stator phase current.

the fifth and seventh harmonic orders: 3.7% and 4.1% of the fundamental component in a five-level waveform compared to 21.9% and 10.3% of the fundamental component in a three-level waveform).

The voltage across the capacitors is shown in Fig. 15 for the same operating condition of Fig. 13, where the phase rms voltage is 100 V [see Fig. 13(a)], $I_{dc}/2$ is about 2.8 A [see Fig. 13(b) and (c)], α is equal to 150° [see Fig. 13(b)]. According to (14), U_{C0} is calculated approximately equal to 420 V

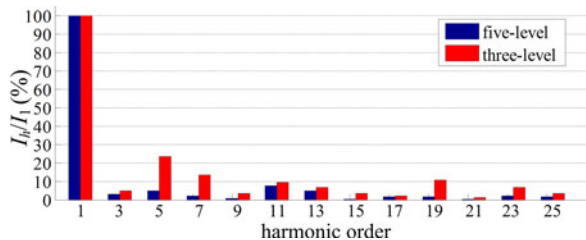


Fig. 14. Percentage of i_{LCIa} and i_a (shown in Fig. 13) harmonic components normalized to the fundamental one.

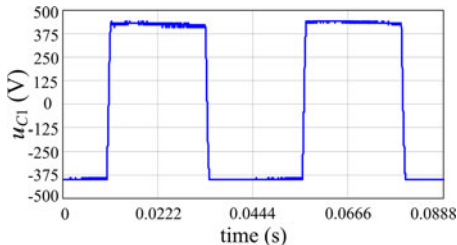


Fig. 15. Experimental waveform of the voltage across the forced-commutation capacitors captured under the same operating conditions of Fig. 13.

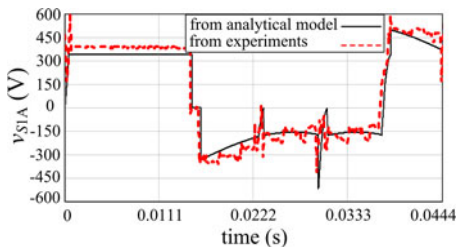


Fig. 16. Experimental and analytical waveforms for the voltage across an auxiliary thyristor, captured under the same operating conditions of Fig. 13.

for this condition, which is in accordance to the experimental results shown in Fig. 15. In addition, the waveform of the capacitor voltage shown in Fig. 15 is the same as the one shown in Fig. 4(a) for u_{C3} .

At the same operating condition, the experimental waveform of the voltage across the auxiliary thyristors is compared in Fig. 16 to the analytical one that is obtained from the explanations presented in [25] (see [25, eqs. (20)–(23)]). A good matching between the waveforms can be found in this figure. The ripples present in the experimental waveform are due to the dc-link current ripples reflected in the resistive and inductive voltage drops, while the dc-link current is assumed to be smooth in [25]. According to the analysis presented in [25] and considering $2 \mu\text{F}$ for the capacitors in the forced-commutation circuit, the rms voltage rating of the auxiliary thyristors is calculated equal to nearly 700 V for the full-load operating condition, i.e., speed of 1000 r/min and rms value of the stator current fundamental component equal to 6.1 A. A voltage of 700 V is reasonable according to the specifications of BT152-800R thyristors.

TABLE II
EXPERIMENTAL DATA

	φ [deg]	I_{dc} [A]	I_f [A]	Stator current harmonics (%)		
				5th	7th	THD
FLCSI	15	5.6	1.8	3.7	4.1	11.5
LCI	30	6.1	2.1	21.9	10.3	26

Furthermore, the current rating of the auxiliary thyristors for the rated working condition can be determined according to (18). Considering that each thyristor in the CSI, $S_1 - S_6$ in Fig. 1, conducts the dc-link current in one-third of a cycle, in order to compare the rated rms current of the auxiliary thyristors with that of the main ones, the value obtained by (18) is normalized by dividing it by $I_{dc}/(2\sqrt{3})$. For this purpose, the quantities t_B , t_1 , and t_2 need to be computed. Assuming $E = 220 \text{ V}$, $I_{dc}/2 = 3.4 \text{ A}$, $\omega = 100 \pi \text{ rad/s}$, and $\alpha = 150^\circ$, t_B is equal to $1.70 \times 10^{-3} \text{ s}$ according to (1). Then, U_{C0} is equal to 475 V using (14) and, consequently, t_1 will be obtained as $2.01 \times 10^{-3} \text{ s}$ by solving (13). Also, t_2 is equal to $2.45 \times 10^{-3} \text{ s}$ according to (12). It should be mentioned that ω' is equal to 3580 rad/s for the forced commutation circuit which, compared to 314 rad/s for the pulsations of the phase voltages, confirms the assumption made in (8). Finally, (18) shows that the normalized rated current of the auxiliary thyristors is equal to 0.28. Despite the short duration of the commutation transient, the auxiliary thyristor must tolerate the dc-link current which could be relatively large. However, this cannot be counted as an issue thanks to the property of the SCRs of being able to withstand large surge currents. For instance, BT152 devices are capable of conducting surge current ten times their rated rms value.

A. Comparison of Experimental Results

In order to highlight the higher performance of the proposed FLCSI versus the conventional LCI, experimental results obtained for the two configurations are summarized in Table II, where φ is the fundamental power factor angle, I_{dc} is dc-link current, and I_f is the WFSM field current.

Comparison of the experimental data reported in Table II shows the benefits brought by the proposed configuration in terms of displacement power factor, dc-link current and therefore motor stator current, motor field current, and motor stator current distortion.

VI. CONCLUSION

A novel SCR-based converter concept is presented in this paper for the supply of high-power WFSM as a high-performance alternative of the traditional LCI. The new concept is based on introducing an additional forced-commutation bridge in parallel to the load-commutated inverter typical of LCI drives. This enables to improve motor current waveform that changes from the usual quasi-square-wave to a multilevel (five-level) shape with reduced harmonic distortion and lower shift angle with respect to motor phase voltages. Resulting benefits can be identified in

a higher power factor, reduced torque ripple, lower field current, and smaller additional and excitation losses. Furthermore, the proposed converter topology is capable of starting the machine with a much better torque than achievable with the usual LCI pulsed operation. An extensive analytical treatment is proposed in the paper to investigate the forced commutation mechanism and to dimension the capacitors and the auxiliary thyristors needed for it. The overall merits of the proposed solution are illustrated by means of numerical simulations in comparative terms with respect to traditional LCI-fed WFSM drives. An experimental set-up based on a small-scale LCI drive prototype has been also prepared and experimental results prove the feasibility and the claimed benefits of the proposed converter system.

APPENDIX A

Next the characteristic data are provided for the equipment assumed in simulations.

Synchronous machine ratings: 1.02 MVA, 570 V, 1034 A, 100 Hz, 4 poles.

Stator circuit parameters: $r_s = 1.8 \text{ m}\Omega$ (resistance), $L_{ls} = 0.07 \text{ mH}$ (leakage inductance), $L_{md} = 0.6316 \text{ mH}$, $L_{mq} = 0.5356 \text{ mH}$ (magnetizing inductances). Field circuit parameters: $r'_f = 0.6 \text{ m}\Omega$ (resistance), $L'_{lf} = 0.0504 \text{ mH}$ (leakage inductance). Damper parameters: $r'_{kd} = 5.1 \text{ m}\Omega$, $r'_{kq} = 8.6 \text{ m}\Omega$ (resistances), $L'_{lkd} = 0.0147 \text{ mH}$, $L'_{lkq} = 0.0243 \text{ mH}$ (leakage inductances).

DC-link inductor: 10 mH.

APPENDIX B

Next the characteristic data are provided for the equipment used in the experiments.

Synchronous machine ratings: 4 kVA, 380 V, 6.1 A, 50 Hz, 6 poles.

Stator circuit parameters: $r_s = 1.45 \Omega$ (resistance), $L_{ls} = 13 \text{ mH}$ (leakage inductance), $L_{md} = 79.2 \text{ mH}$, $L_{mq} = 49 \text{ mH}$ (magnetizing inductances). Field circuit parameters: $r'_f = 189 \text{ m}\Omega$ (resistance), $L'_{lf} = 3.33 \text{ mH}$ (leakage inductance). Damper parameters: $L'_{lkd} = 9.6 \text{ mH}$, $L'_{lkq} = 13.5 \text{ mH}$ (leakage inductances).

DC-link inductors: 78 mH.

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