A scalable High Voltage Power Supply System with system on chip control for Micro Pattern Gaseous Detectors

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ABSTRACT

The requirements posed to high voltage power supply systems by the operation of Micro Pattern Gaseous Detectors are specific in terms of high resolution diagnostic features and intelligent dynamic voltage control. These requirements are needed both when technology development is performed and when extended detector systems are supplied and monitored. Systems satisfying all the needed features are not commercially available.

A single channel high voltage system matching the Micro Pattern Gaseous Detector needs has been designed and realized, including its hardware and software components. The system employs a commercial DC/DC converter and is coupled to a custom high resolution ammeter. Local intelligence, flexibility and high speed inter-connectivity are provided by a System on Chip Board and the use of a powerful FPGA. The single channel system has been developed, as critical milestone towards the realization of a multi-channel system.

The design, implementation and performance of the system are reported in detail in this article, as well as the performance of the single channel power supply when connected to a Micro Pattern Gaseous Detector in realistic working condition during a test beam exercise.

1. Introduction

Gaseous detectors are fundamental components at many present and future frontier particle physics experiments, in particular when large volumes have to be instrumented or when low material budget is required. The novel Micro-Pattern Gas Detector (MPGD) concepts, namely Gaseous Electron Multiplier (GEM) [1], Micromegas [2] and, more recently, other MPGD schemes, have overcome the limits of the previous gaseous detectors technologies as wire-chambers, drift tubes, and others. These new radiation detectors and imaging devices with unprecedented spatial resolution, high rate capability, large sensitive area, stable high-gain operation and excellent radiation hardness are already being employed, while further developments are ongoing [3]. Covering large areas with MPGDs is one of the main motivations for these developments: about 1200 m^2 of resistive bulk Micromegas for the New Small Wheel (NSW) muon stations of ATLAS are needed [4], about 1000 m^2 of GEM foils for the upgrade of the CMS muon system are under construction [5], the ALICE experiments will massively employ this technology for the novel sensors of its large TPC [6].

A common need of MPGDs is the request of biasing the device electrodes at different voltages, up to several kV. In case of large area applications, electrode segmentation cannot be avoided. In fact, the energy accumulated in couples of nearby electrodes, for instance the two faces of a GEM foil, is proportional to the electrode surface; when a discharge occurs the stored energy is completely dissipated by the formation of an electric arc between the electrodes. Surface segmentation results in a reduction of the dissipated energy preventing possible detector damage. Moreover, thanks to segmentation, the discharge event causes a local transient inefficiency of the detector, namely the interested sector, and not of the whole surface. The downside of this approach is a larger number of independent High Voltage (HV) channels, which may result in a non negligible increase in the project costs, in connector space requirements and in cabling deployment. A

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compromise solution is by grouping HV channels, while introducing decoupling resistors. The system flexibility is then reduced and the capability of localizing defective areas is degraded. Furthermore, the typical time resolution of current and voltage measurements of commercial power supplies is in the order of milliseconds, namely totally inadequate to study the propagation of discharges phenomena among different electrodes and areas of the detector. This poor time resolution limits the possible diagnosis of faults in the detectors and prevents the study of the discharge mechanisms.

This article is dedicated to the development of a single-channel High Voltage Power Supply System (HVPSS) suited for the MPGD technologies. The single-channel HVPSS is the needed initial step towards the realization of multichannel systems.

2. Specifications of the High Voltage Power Supply System for MPGDs

The development of an HVPSS suited for the MPGD technologies originates from the experience gained in upgrading COMPASS RICH-1 with MPGD-based single photon detectors [7], preceded by seven years of dedicated research and development. The project goal is matching all the requirements for the complete monitoring and the accurate handling of MPGDs, also those that cannot be answered using commercial power supply systems. A second goal is to provide a tool to perform MPGD R&D, often requiring monitoring of the voltage and current parameters with fine time resolution, namely measured values coupled to timestamps with ns resolution. This feature is necessary in order to understand the precise evolution of the discharge phenomena as well as the presence of pre break-down conditions. The possibility to prevent and limit discharge events requires the use of local re-configurable intelligence for the application of feedback protocols and the broadcast of the information to neighboring independent channels, when user defined conditions are matched. The fast control of the HV channels is a key ingredient to exploit the cut off of the HV power supply.

Relevant design figures of the HVPSS derive from the requirements illustrated above: precise current monitoring with 10 pA resolution at a sampling frequency higher than 100 kHz, HV monitoring with resolution better than 0.5 V up to 4 kV at sampling frequency greater than 100 kHz and a time stamp precision of 10 ns for the voltage and current measurements. Finally, a reconfigurable on board logic is required, which includes two categories of actions dedicated to condition the supplied voltage, namely time critical and time non-critical ones, as detailed in the following.

The requirement to perform current measurements with fine resolution for electrodes with voltage level up to 4 kV has implied non-trivial choices during the development and prototyping of the instrument especially for what concerns the insulation properties of the device components. Two relevant design choices are related to these requirements: HVPSS is powered via 12 V lines and data are transferred via optical fibers for galvanic insulation and to prevent the propagation of the electronic noise via the ground lines.

Finally, the HV has to be generated at the detector location to reduce the parasitic capacitance of connectors and cables. For this purpose, the system is realized with a compact design to limit the space occupancy.

3. The High Voltage Power Supply System

The first step of the HVPSS development is the definition of the logic blocks and their inter-connectivity as well as the identification of the main hardware components. The resulting scheme is illustrated in Fig. 1 where the arrows indicate the data-flow directions. The identified elements can be listed as follows:

1. the DC/DC converter (Section 3.1);
2. the picoammeter board (pA) (Section 3.2);
3. the data acquisition board for high speed Analog to Digital Conversion (ADC) of the data (Section 3.3);
4. the data acquisition carrier based on a System on Chip (SoC) device (Section 3.4);
5. the Digital to Analog Converter (DAC) used to condition the HV power supply (Section 3.5);
6. the ADC board acquiring and analyzing signals from the external sensors (Section 3.6);
7. the external sensors (Section 3.6);
8. the network interface via optical fiber.

In total eight main blocks have been identified. Each logical block has a correspondent physical one: this choice is based on two motivations. Firstly, in case one component gets damaged during operations it can be easily replaced with a minimal intervention on the system; secondly, if a more performing version of a component in any of the blocks becomes available, it can be easily implemented. The design strategy has already paid off: the DC/DC converter block, which is in charge of the HV supply, is going to be replaced with a novel one, making use of a more performing converter, which became available only recently.

3.1. The DC/DC block

The three main characteristics driving the choice for the high voltage power generator are:

- compactness, related to space requirements;
- capability to provide both positive and negative voltages;
- the noise figures affecting the generated HV.

The market investigation has pointed out the candidate devices listed in Table 1.

An interesting aspect of the EMCO[2] devices is their compactness and their availability in SMD-like package for direct mounting on PCBs. The ISEG[3] devices are less compact, as visible in Fig. 2. The entire Q60, A60, AG60 families by EMCO and the BPS family by ISEG have been studied. The minimum V_{Out} of each device, indicated as V_{Th} has been measured. For this purpose, a PCB board hosting a 100 MΩ resistor OHMITE MX load has been connected to the output of each unit. The devices under test are powered with a TTI[4] PL320QMD power supply unit. The low input control voltage, namely the V_{Ctrl} is measured via a multimeter while the HV output is monitored both via a HV probe FLUKE[5] 80K-6 and via a second multimeter connected to a 1:1000 calibrated resistive divider. The measured V_{Th} is 920 V for the Q60 devices, 1500 V for the AG60 devices and 600 V for the A60 devices. The lowest output voltage was obtained for the ISEG converters with a minimum measured voltage of 1 V. It is important to remark that, during operation, all the EMCO devices exhibit discharge events with a frequency apparently correlated to the temperature of the device, which increases during operation. No discharge events have been detected for both the ISEG converters.

A preliminary analysis of the noise structure of the devices has been carried out via the Fast Fourier Transform (FFT) function on the oscilloscope. The noise performance of the devices are studied in a more detailed way using a spectrum analyzer with a 50 Ω terminated probe connected in series to the 100 MΩ resistor. The noise spectra refer to an output voltage of −4 kV for all the modules. Examples of noise spectra are provided in Figs. 3 and 4 for the converters Q60N-5R by EMCO and BP40105n12 by ISEG, respectively. The performance of the ISEG device is superior, as no noise peaks can be observed. The ripple

[2] EMCO High Voltage, Sutter Creek, California USA.
[3] ISEG, Bautzner Landstr. 23, Radeberg, Germany.
[4] Aim and Thurlby Thandar Instruments, Glebe Rd, Huntingdon, Cambridgeshire, PE29 7DR, United Kingdom.
[5] Fluke Corporation, Everett, Washington, USA.

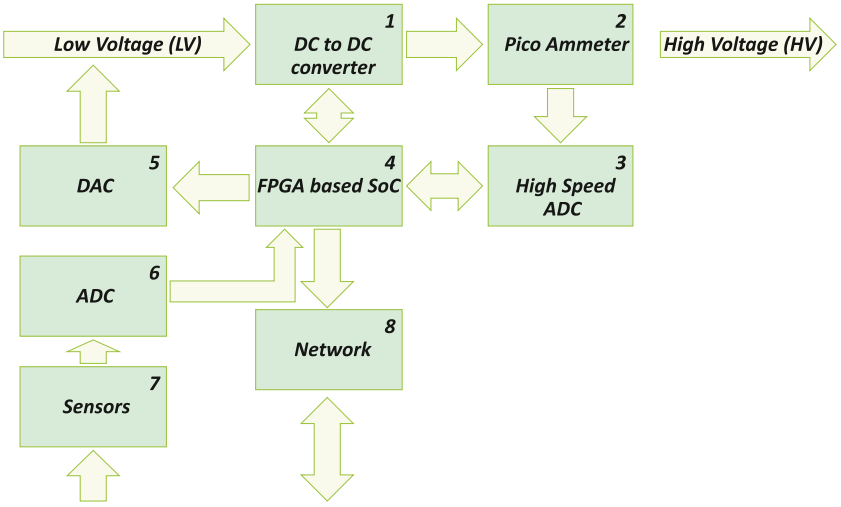

Fig. 1. General block diagram of the control system for a single unit high voltage power supply. The HVPSS sub systems are shown and the inter-connectivity of the different elements is indicated by the arrows.

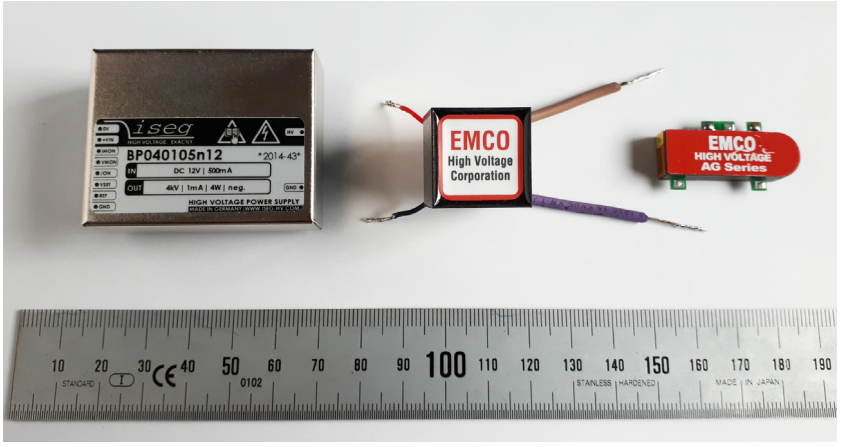

Fig. 2. Image of some the DC/DC converters studied: left the BP40105n12; center the Q60-5R; right the AG60P-5.

Table 1
Main parameters of the candidate DC/DC converters. These devices are produced by EMCO and ISEG.

DC/DC converter	Producer	V_{Out} [kV]	V_{Ctrl} [V]	Power [W]	Ripple	Dimensions [mm^3]
Q60-5R	EMCO	0 to +6	0 to +5	0.5	<1.0%	13.72 × 13.72 × 13.72
Q60N-5R	EMCO	0 to −6	0 to +5	0.5	<1.0%	13.72 × 13.72 × 13.72
A60P-5	EMCO	0 to +6	0 to +5	1	0.15%	11.43 × 23.37 × 6.35
A60N-5	EMCO	0 to −6	0 to +5	1	0.15%	11.43 × 23.37 × 6.35
AG60P-5	EMCO	0 to +6	0 to +5	1	0.3%	17.50 × 26.70 × 6.35
AG60N-5	EMCO	0 to −6	0 to +5	1	0.3%	17.50 × 26.70 × 6.35
BP40105n12	ISEG	0 to −4	0 to +5	1	<20 mV	40 × 50 × 17
BP10105p12	ISEG	0 to +1	0 to +5	1	<20 mV	40 × 50 × 17

noise of Q60N-5R can be seen in Fig. 5, clearly showing its periodicity and its nearly 20 mV peak to peak amplitude. A similar behavior is observed for the other converters by EMCO. ISEG devices exhibit lower noise level and no ripple enhancement at fixed frequency. Well defined frequencies were observed in the noise power spectra for all the EMCO converters of the Q60, A60P and AG60P families: they contribute to the output voltage ripple. Finally, it must be noticed that the EMCO devices have no voltage neither current monitor pins, on the contrary provided in the ISEG devices.

The ISEG DC/DC converters have been selected on the base of the studies described in this section. Their good performance is most probably related to the special resonance converter technology and the moulded metal box shielding, which guarantee low electromagnetic interference and low ripple and noise.

The response characteristics of the selected converter have been studied by measuring both the output voltage via a Lecroy[6] PPE20kV HV probe and the output voltage of the V_{mon} pin via a Keytley 197A $5\frac{1}{2}$ digit resolution digital voltmeter[7] as function of the applied V_{Ctrl} voltage. The last one is controlled via a 16 bit DAC MAX5216 where the Less Significant Bit (LSB) corresponds to 300 mV variation of the HV output (more details about the DAC are provided in Section 3.5).

[6] Teledyne Lecroy, Chestnut Ridge, New York, United States.
[7] Keithley Instruments, Cleveland, Ohio, USA.

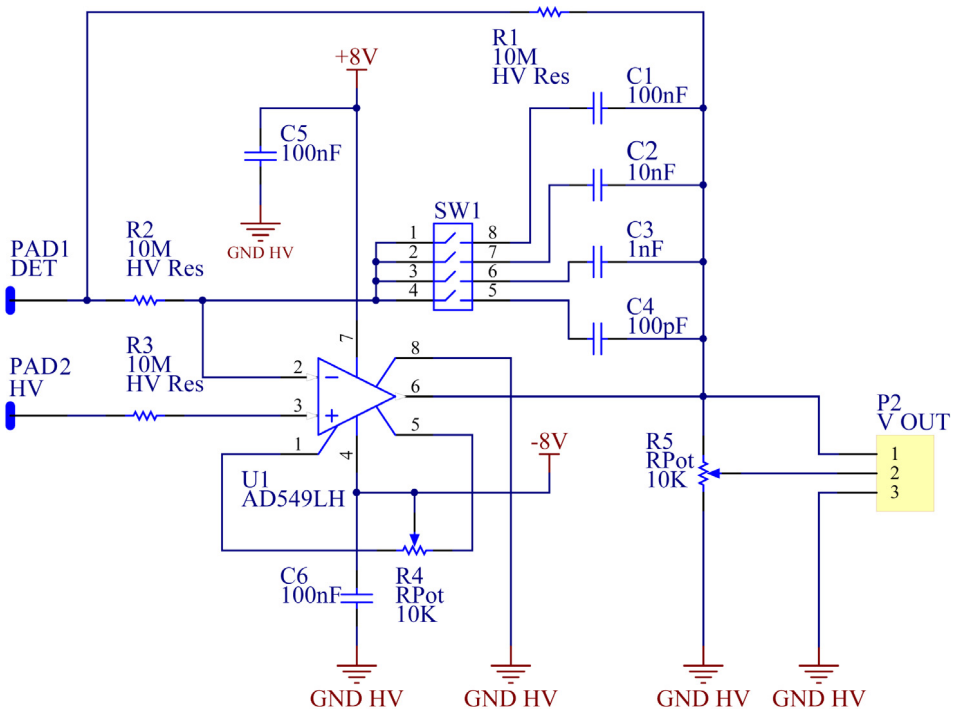

Fig. 9. Schematics of the ammeter board with the main components of the current to voltage converter.

Fig. 10. Picture of the ammeter board with components installed ready for the preliminary functional tests.

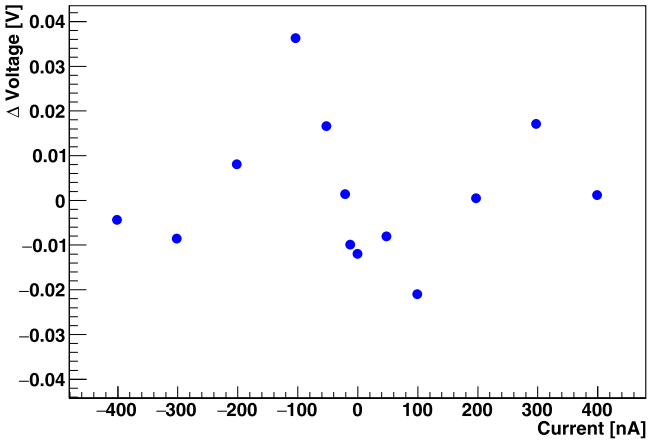

Fig. 11. pA board characterization: Difference of output voltage with respect to the expected valued versus input current in the ±400 nA range. The expected value is extracted from the linear fit of the data.

3.2. *The picoammeter board*

The pA board, Fig. Fig. 10 can be divided into two main functional sub-blocks: the current to voltage converter (I/V) and the power supply system. The I/V converter is based on an operational amplifier in trans-conductance mode [8,9] (Fig. 8). The voltage output v_o is related to the input current by the relation $v_o = R_b \cdot i_i$. Our implementation exploits the capability of the AD549LHZ by Analog Devices[8] operational amplifier capable to operate with ultra-low input bias current. The amplifier is coupled to a high precision feedback resistor to define the current/voltage gain. The pA board schematics is presented in Fig. 9. An input current of 100 nA generates an output voltage of 1 V, being the feedback resistor (R_1) of 10 MΩ. The noise affecting to output voltage is limited and filtered by several capacitors added via dip switches in parallel to R_1.

An adjustable trimmer is used for the fine regulation of the offset (R_4) as well as a second one at the exit of the I/V converter to match the input ADC range (R_5). Several passive components, resistors and diodes (R_2, R_3, D_4, D_5, D_6 e D_7), have been added to protect the device from the discharges that may occur at detector level in order to avoid possible damages.

The pA board is supplied by a dedicated ultra-low noise voltage powering. The low voltage feeding circuitry uses two DC/DC converter units with high insulation properties by RECOM.[9] The first converter, dedicated to the AD549LHZ, provides ±12 V via the REC6-1212DRW/10/A, the second one provides 5 V and a maximum current of 1A for the ADC board services via the REC6-1205SRW/10/A. The two voltage outputs of the DC/DC converters are filtered and stabilized via two voltage regulators at ±8 V. Two Zener diodes protect the operational amplifier from the voltage peaks associated to the discharges of the detector.

A coarse calibration measurement has been performed on a large current range ±400 nA to verify the pA linearity. A power supply unit via a 50 MΩ resistor has been used as controlled current source.

[8] Analog Devices, https://www.analog.com.

[9] RECOM https://recom-power.com.

Table 2
Measurement of the current: effective number of bits, effective sample rate and resolution error for a current range of ±30.6 nA versus the decimation factor.

N	n_b	Effective sample rate (MHz)	Theoretical resolution Δ (nA)	Theoretical quantization error $\sqrt{\Delta^2/12}$ (nA)	Experimental statistical error σ (nA)
2	8.5	250.00	84.4	24.4	65.2
4	9	125.00	59.7	17.2	58.8
16	10	31.25	29.8	8.6	13.6
64	11	7.81	14.9	4.3	7.0
256	12	1.95	7.5	2.2	6.6
512	12.5	0.98	5.3	1.5	3.9

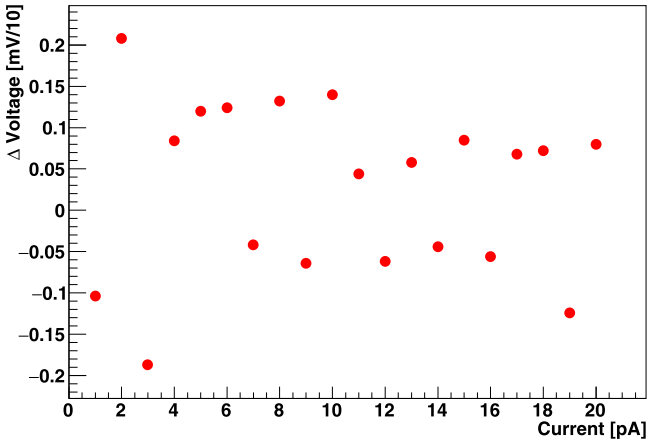

Fig. 12. pA board characterization: Difference of output voltage with respect to the expected valued versus input current in the 0–20 pA range. The expected value is extracted from the linear fit of the data.

The current is measured via a Keytley 6485 picoammeter. The output voltage of the operational amplifier has been monitored via a multimeter.

The results are reported in Fig. 11 and show the good linearity of the I/V converter over the full range. The data points there plotted are the difference of the measured values with respect the expected value from a linear fit of the same data. The measurement has been repeated in the reduced range 0–20 pA of the input current to confirm the linear response also in the region of very low currents, near to zero, as illustrated in Fig. 12. A good linear response is observed.

3.3. Data acquisition mezzanine board

The ADC board is in charge of the fast digitization of the voltage signal from the transconductance amplification stage to measure the HV supply current. The detection of fast transient phenomena (e.g. spontaneous electrical discharges) with ns time-resolution is one of the characterizing requests for HVPSS. To meet these requirements, a low power 8-bit high speed 500 MSPS ADC08500 analog to digital converter by Texas Instruments[10] was selected.

The ADC board shown in Fig. 13 is equipped with a Low Pin Count (LPC) FMC connector (ANSI VITA 57 standard) and it has been designed to fully exploit all the main characteristics of the selected ADC. This includes self-calibration, fine adjustment of the input full-scale range and offset and multiple ADC synchronization capability.

Three on board power regulators are implemented for reliable and low noise operation; protection circuits are present to avoid damages to the ADC due to out-of-range voltages and spikes.

The ADC has a 1:2 demultiplexer that feeds two low-voltage differential signaling (LVDS) buses. Therefore, the output data frequency on each bus is reduced to half the sampling rate. The digital output consists of 32 physical lines implementing 16 LVDS pairs operated at 250 MHz. Three other LVDS lines are provided: the input clock, the output clock, and a fast out-of-range signal.

The analog input signal is single ended and DC coupled. It is converted to a differential signal by a high speed differential line driver.[11] The driver architecture foresees the independent setting of the input and output common mode voltage. This feature simplifies the interface to the differential inputs of the ADC. The optimum performance of the ADC is also granted by connecting the ADC output common mode voltage to the corresponding reference input pin of the driver.

A self-calibration procedure can be performed at power-up and also at any time upon user's command. This procedure minimizes full-scale and offset errors and improves the differential and integral linearity. Therefore, the procedure maximizes the signal to noise ratio and the number of the effective ADC bits. The ADC has the capability to reset its sampling activity at a well defined time upon a specific signal. It is also possible to synchronize the data output, in a multiple ADC system where a common clock is distributed.

3.3.1. Oversampling and decimation

The ADC is continuously sampling the picoammeter output at the maximum rate of 500 MHz. The data stream is buffered in the FPGA. The minimum design requirement is providing current measurements with a resolution of 10 pA at a sampling rate of approximately 100 kHz. This requirement is matched by applying the oversampling method implemented in the FPGA firmware. N 8-bits samples collected at 500 MHz rate are accumulated in order to produce every $2N$ ns an effective sample of n_b bits according to Eq. (1):

$$n_b = \left(8 + \frac{1}{2} Log_2 N\right) \tag{1}$$

The resulting resolution depends on n_b, which varies versus the decimation factor N, and the ADC dynamic range. The effective resolution and sampling rate versus the decimation factor for a ±30.6 nA current range are presented in Table 2.

A comparison between the theoretical quantization error and the experimental statistical error attainable when applying decimation versus n_b is presented in Fig. 14. The system provides 3.9 pA resolution at approximately 1 MHz sampling frequency for N=512; with this decimation choice, there is no major difference between the theoretical and experimental error values.

Several test as well as calibration measurements have been performed in order to exclude performance limitations due to impedance matching and noise propagation from the digital to the analog domain of the pA board and the data acquisition mezzanine board. An example is provided in Fig. 15, where the ADC calibration for static input current measured at a sampling frequency of 2.6 kHz is presented. The system linearity is not affected and there is no evidence of digital noise effects.

[10] Texas Instruments Incorporated 12500 TI Boulevard Dallas, Texas 75243 USA.

[11] Texas Instruments, LMH6555.

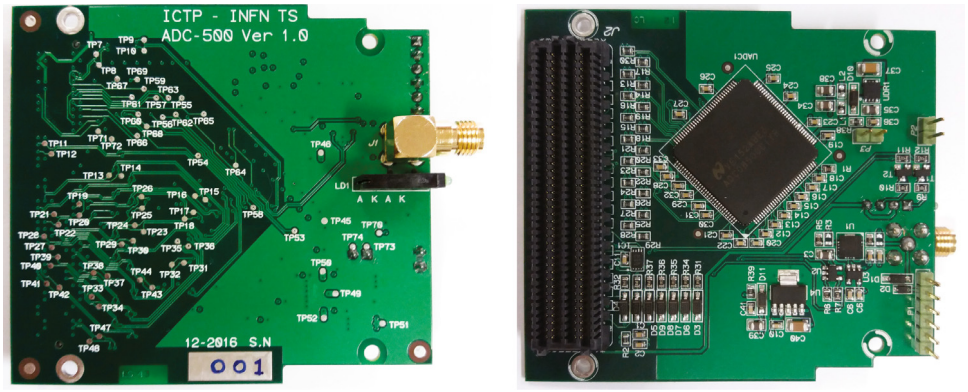

Fig. 13. The ADC board hosting the ADC08500, rear side (left) and front side (right). The low pin count FMC connector is clearly visible.

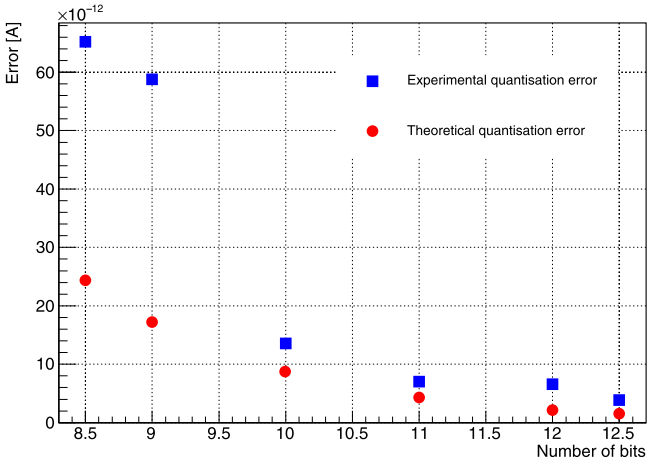

Fig. 14. Theoretical quantization error and experimental statistical error versus n_b.

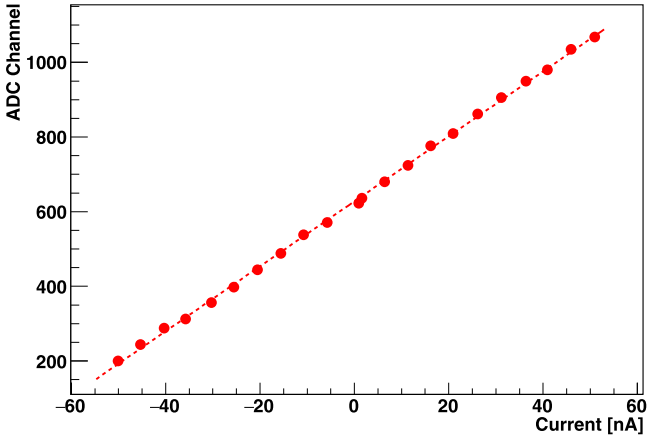

Fig. 15. Calibration of the ADC board hosting the ADC08500 and the pA board for static input current in the ±50 nA range. The line is the result of a linear fit to the data.

3.4. FPGA based SoC

The SoC FPGA board selected for prototyping and software development purposes is the ZedBoard.[12] The choice is based on the analysis of the resources required by the system design tasks. The ZedBoard is based on the modern hybrid fully-programmable System-on-Chip (SoC) device Zynq-7020, which combines a 'hard' dual core ARM Cortex-A9 processor with an Artix-7 FPGA fabric. The SoC manages the ADC, performing a fast post processing of the data to tag those events whose digitized waveforms are saved and sent via Ethernet for offline data analysis. It also controls the HV output, applying the fast and the slow HV settings. The latter takes also in account the environmental conditions, namely external pressure and temperature (Section 3.6).

After a first stage of development, which proved the correct choice of the SoC device, the need to reduce the physical size as well as the possibility to use open hardware, suggested the adoption of a custom carrier designed by the Argentinian National Institute of Industrial Technology (INTI). The adopted board, namely CIAA-ACC is an open hardware high pin count (HPC) FMC carrier (ANSI VITA 57.1 standard) based on a Zynq-7030 [10] shown in Fig. 16.

3.4.1. The HVPSS control

The control activity of the HVPSS is shared among three main subsystems: the FPGA, the microprocessor and the control PC. The FPGA subsystem is in charge of time-critical tasks, the microprocessor subsystem handles the communication between the PC and the FPGA, and others non time-critical tasks. The PC is the operator interface used to setup and monitor the system via a custom Graphical User Interface (GUI). It also handles data storage. The microprocessor and the PC are interconnected through a dedicated point-to-point Gigabit Ethernet link.

3.4.2. FPGA subsystem

The logic cores designed for data handling and control implemented in the FPGA subsystem are shown in Fig. 17. The main tasks are time *stamping and raw sample acquisition, signal analysis and diagnostics, peripheral control and FPGA-Processor communication*. The time critical tasks are performed by the use of custom logic blocks.

The reference timing of the system for global synchronization is generated by an IIC Real Time Clock (RTC) in a *Timestamp Generator* at 1 Hz frequency, which provides the slow clock (sclk). The fast clock (fclk) at 500 MHz is generated by the FPGA to control the ADC sampling. A second fast clock signal at 250 MHz is produced to manage the ADC data output. The fclk is combined with the sclk to obtain an absolute time stamp with 2 ns resolution. The time synchronization process is illustrated in Fig. 18. This logic block associates the correct time stamp to the triggers. With this scheme the maximum synchronization error is one fast-clock cycle.

The raw data from the ADC are stored on a *data buffer* logic block based on a RAM shift register with configurable delay, which receives input when a trigger condition is detected. The *sample manager* logic block creates a package featuring a configurable number of samples before and after the trigger to be stored on a FIFO with the timestamp information corresponding to the trigger. The detection of trigger conditions is discussed in Section 3.4.5.

[12] https://www.xilinx.com/products/boards-and-kits/1-8dyf-11.html

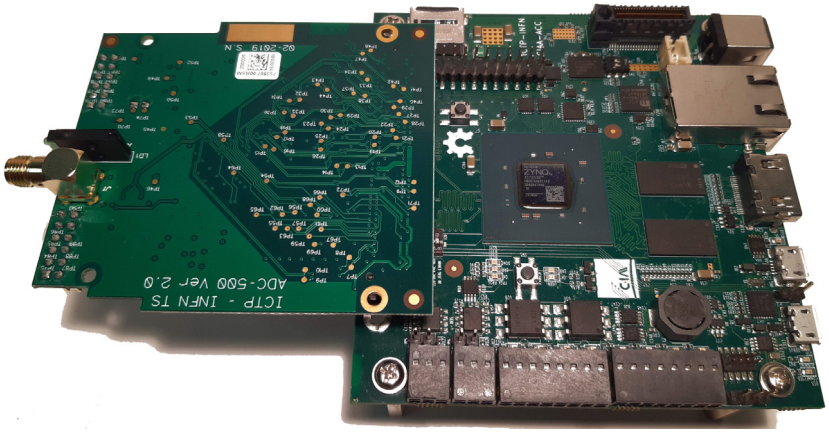

Fig. 16. The Zynq-7030 CIAA ACC board connected to the ADC Mezzanine board.

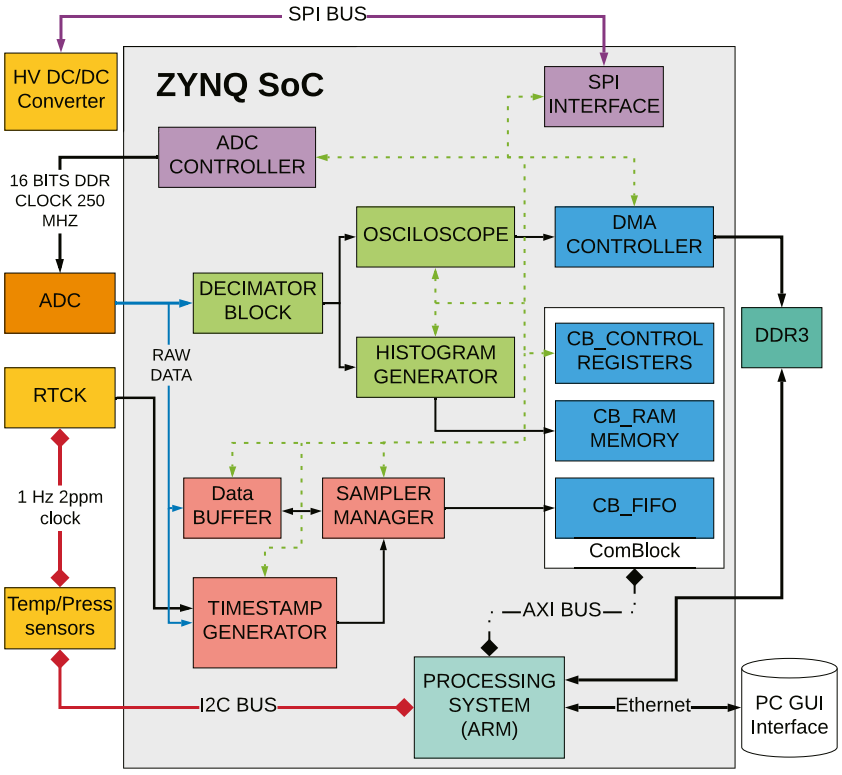

Fig. 17. Schematics of the FPGA subsystem and its interactions with the processor and the dedicated hardware peripherals.

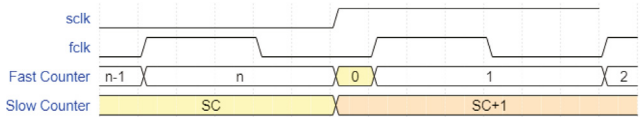

Fig. 18. Time synchronization process.

The data stream from the external ADC is continuous. Oversampling and decimation of the these data are by the *Decimation* logic block, where the number of input samples can set by the user. In this way, an output data stream with lower data rate is produced with reduced effective sampling frequency and with increased amplitude resolution (Section 3.3). The decimated data are locally analyzed in the *diagnostic* logic block, in order to produce a histogram of the amplitudes collected during a predefined acquisition time. In parallel, the histogram and a continuous segment of the decimated data is transferred to the PC. The *histogram* logic block uses a RAM memory to generate samples histograms by using the RAM address as bin number: stored value is read and increased by one unit. This blocks needs three clock cycles and requires a write enable to perform a bin increase. When the preset number of samples is reached, a *done* signal is raised. The histogram can be set and cleaned by software. Moreover, a continuous segment of decimated data is stored on a FIFO and transferred to the processor by direct memory access (DMA). An *Oscilloscope* logic block features an edge detector trigger mode or auto trigger.

A *communication* logic block (ComBlock) IP core [11] is used to connect the processor with the FPGA. This IP block is an interface between the processor and the FPGA. Its role is to hyde the complexity of any specific bus by providing a simple access to the generic registers of a True Dual Port RAM (TDPRAM) and an asynchronous FIFO.

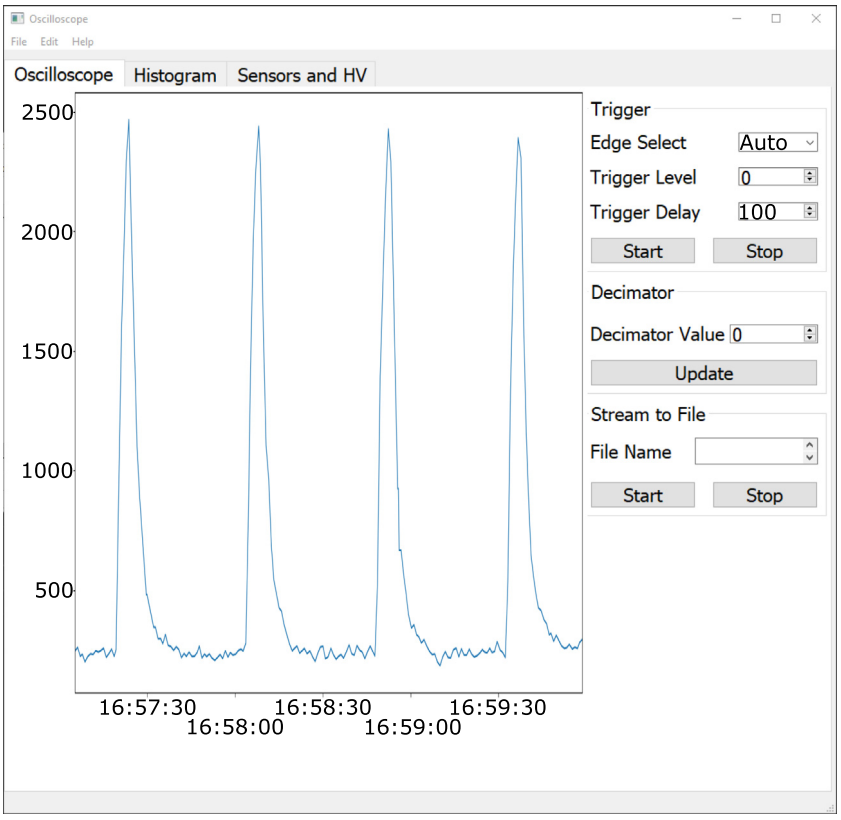

Fig. 19. GUI oscilloscope tab: the measured current in pA and the control parameters from the FPGA Oscilloscope block.

Galvanic insulation between the HVPSS and the ethernet network is obtained via MCM110SC2EU,[13] a Multi Mode Fiber Ethernet Media Converter, enabling the safe operation of the remote monitoring and preventing any noise propagation from and to the device thanks to the insulation properties of the optical fiber.

3.4.3. Microprocessor subsystem

The microprocessor manages, as already anticipated, the FPGA-subsystem, provides ethernet connection to the board and handles non time critical peripherals through an IIC interface. The power supply voltage and current monitored values are logged at 1 Hz rate. The voltage corrections to preserve the detector gain when environmental parameters change (Section 3.6), are calculated and applied by the microprocessor.

The correction algorithm depends on the detector characteristics and it is the result of dedicated laboratory tuning exercises. An example is provided in [12], where the following correction equation is introduced:

$$V(P,T) = V_0\left(1 + 0.5\left(\frac{P}{P_0}\cdot\frac{T_0}{T} - 1\right)\right) \tag{2}$$

where V is the voltage, P is the absolute pressure, T is the absolute temperature in degrees Kelvin and V_0, T_0 and P_0 refer to reference conditions. $V(P,T)/V_0$ is the compensation factor.

An Application Program Interface (API) is built in the microprocessor to handle the configuration and readout routines of the different instruments in the system. This API is accessed by a communication server built in a real time operative system (freeRTOS) exchanging the data packets to the PC. A high speed Ethernet connection (1Gbit/s) has been implemented in the processor using the lightweight TCP/IP stack (lwIP library).

[13] https://www.startech.com

3.4.4. PC control and Graphical User Interface GUI

The system is controlled from a PC by a graphical user interface (GUI) written in PyQT. The GUI uses the API of the microprocessor and organize the control of the different instruments in tabs. Moreover, all the data from the HVSPP can be stored in the PC for further analysis.

The GUI, in its current version, is divided in three tabs:

- Oscilloscope tab: Provides a mean to control and visualize decimated data coming from the ADC. Standard oscilloscope tools are provided such as edge select, trigger level and trigger delay. Scale parameters can be set and adjusted by using contextual menus. (Fig. 19).
- Histogram tab: Sets the number of data points and starts the generation of the histogram inside the FPGA. It informs the user about the state of the generation by a progress bar display of the count. It shows the generated histogram in a graphical form similar to the example provided in Fig. 20. The histogram has three capture modes:
  - Single capture, displays the histogram once the data points count is reached.
  - Continuous mode, displays and generate a new histogram each time the count is reached cleaning the previous one.
  - Cumulative mode, generates a new histogram in continuous mode without cleaning the previous histogram information.
- HV and sensors tab: This tab displays the pressure and temperature information from the dedicated sensors and a history log for each. The HV V_0 value can be set in this tab as well as the T_0 and P_0 parameters to calculate the compensation factor Eq. (2). The voltage and the HV correction can be enabled by the buttons on the display. (Fig. 21).

3.4.5. Discharge tagging

In case of an electrical discharge, it is important to precisely measure the event time, while the resolution of the current monitoring

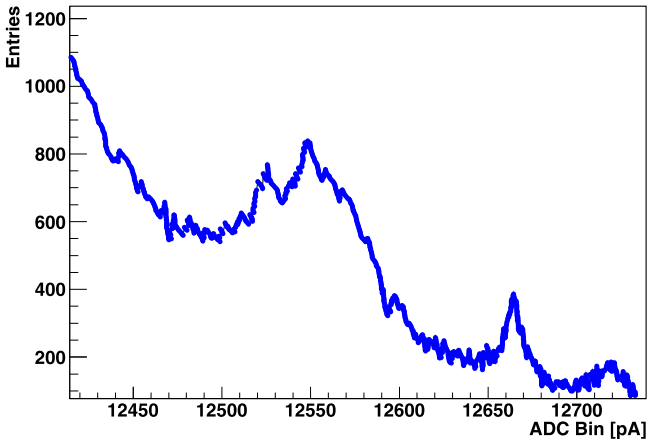

Fig. 20. Amplitude histogram generated in the FPGA Block with ADC bins converted in pA.

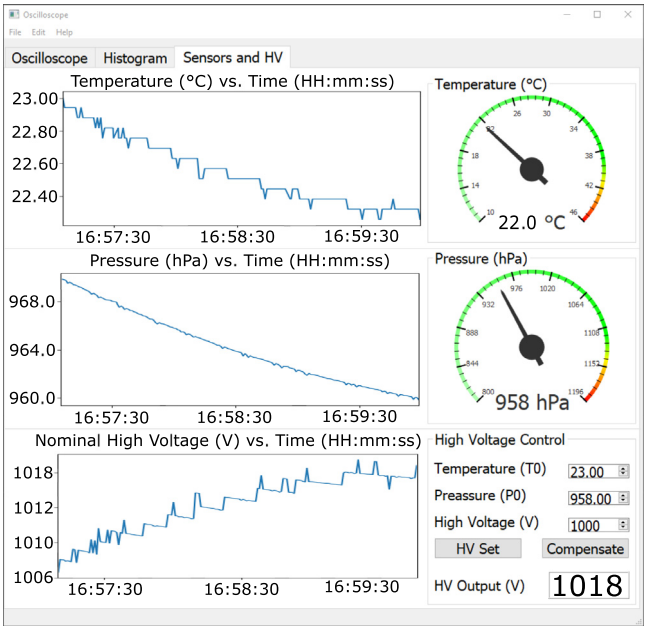

Fig. 21. GUI HV and sensors tab: temperature log in celsius, pressure log in hPa and compensated voltage log in volts.

can be relaxed. Despite the limited bandwidth of the trans-conductance amplifier of the picoammeter board, these transient perturbations are large and fast enough to propagate through parasitic paths till the output where they are detected with 2 ns time resolution.

The raw data input signal from the ADC is stored in a circular buffer allowing to save a number of samples before the event. When a trigger condition happens the buffered data and a number of samples after the event are tagged and stored on a FIFO. Each tag is packed on the FPGA and includes the information about the event number, the number of samples stored before and after the trigger, the event timestamp information and the whole stored data.

3.5. DAC

The voltage control is via the optodecoupled PMOD 16 bit DAC MAX5216 by Maxim Integrated[14] providing the reference voltage to the DC/DC converter. The selected optodecoupler is controlled by a 3 wire

[14] https://www.maximintegrated.com

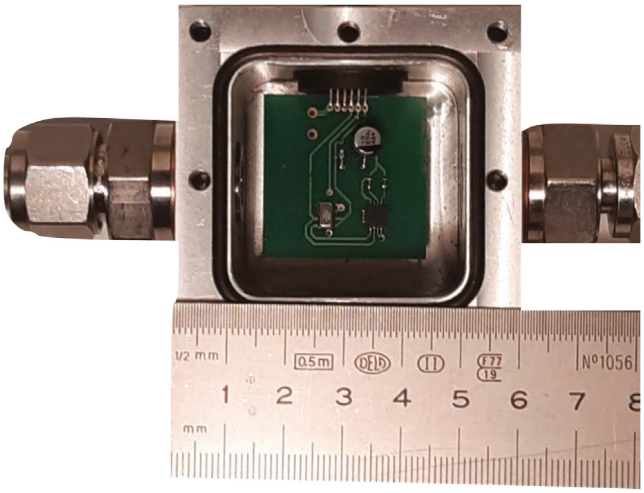

Fig. 22. The PCB board hosting the pressure and temperature sensors, hosted in a gas tight box in series with the gas supply line.

SPI interface and can handle clock frequencies up to 50 MHz. The DAC output is buffered resulting in a low supply current of 80 μA and a low offset error. A zero level applied to the CLR pin asynchronously clears the contents of the input and DAC registers and sets the DAC output to zero independently of the serial interface. One of its interesting features is a safe Power On Reset (POR): it provides a zero DAC output at power-up. It allows for a minimum voltage step adjustment of ≈300 mV when coupled to the ISEC DC/DC converters.

3.6. Pressure and temperature sensors

The reading and calibration compensation of the pressure and temperature sensors described in Section 3.6, are directly managed by the microprocessor without the intervention of the FPGA. This values are periodically read and processed by the microprocessor for monitoring and slow control purposes.

The temperature (T) and pressure (P) are important parameters in gaseous detectors: in fact, the detector gain depends on them, while a constant detector gain is a must to guarantee stable performance. It has been demonstrated that gain stability at the level of a few percent can be maintained over months, even in a multi-amplification stage detector, when the applied voltage is adjusted to compensate P and T variations [12]. The HVPSS has been design to ensure the automatic adjustment of the HV output to compensate for T and P variations.

The temperature and pressure values are obtained by the ADT7420 by Analog Devices and MS5611-01BA03 by TE Connectivity Measurement Specialties[15] sensors, respectively. Both sensors are mounted on an external PCB board (Fig. 22), designed to be easily inserted into the gaseous detector volume or in series with the gas flow line, near the detector input or output. ADT7420 is a high accuracy digital IIC temperature sensor. It includes an internal band gap reference and a 16-bit ADC to monitor and digitize T with 0.0078 °C resolution. This sensor is rated for operation in the −40 °C–+150 °C T range without requiring any correction or calibration by the user.

MS5611 is an integrated digital pressure sensor with SPI and IIC bus interfaces, the second one used in our application. The sensor includes an ultra low power 24 bit $\Delta\Sigma$ ADC with internal factory calibrated coefficients, calculated and stored in a 128-bit internal PROM. After the conversion command used to initiate uncompensated pressure and uncompensated temperature measurements, a read ADC command is

[15] https://www.digikey.ch/en/supplier-centers/t/te-connectivity-measurement-specialties

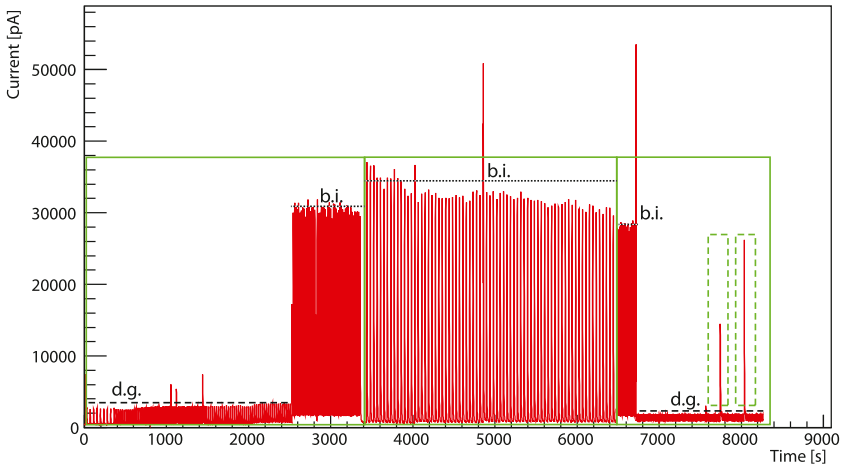

Fig. 23. The current versus time as measured by the HVPSS at the test beam, where the detector was experiencing different beam setting condition and detector working parameters. The areas in the three rectangles highlight the different beam duty cycle, the dotted lines marked with the letters b.i. correspond to different beam intensity conditions, the dashed lines marked with the letters d.g. correspond to different detector operating conditions, the areas in the dotted rectangles highlight two examples of high current surge related to detector discharges.

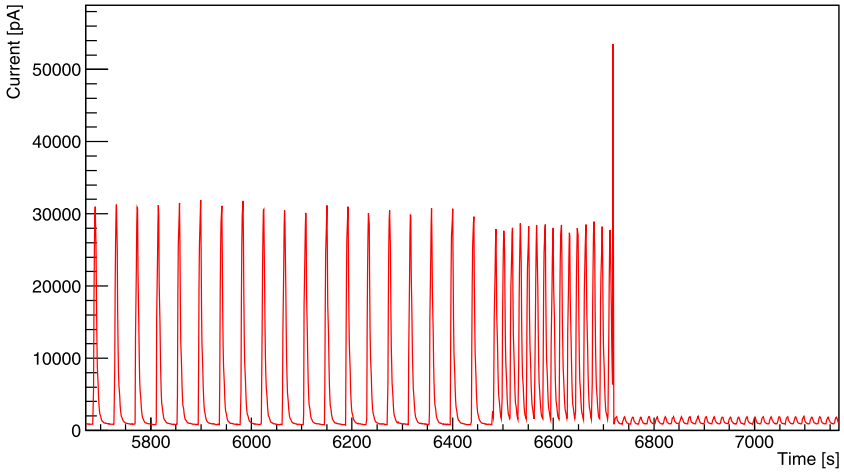

Fig. 24. A zoomed view of a portion of Fig. 23. The variation of the beam duty cycle and of its intensity can be clearly appreciated.

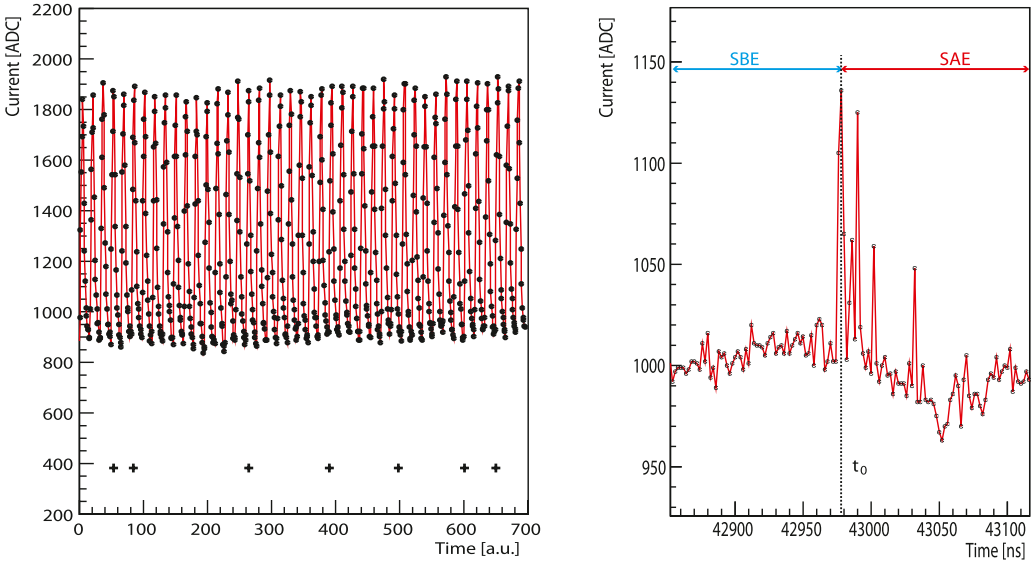

Fig. 25. Measured current versus time. Left: the black dots are the measurements obtained applying the n factor, the read line interpolates them, the cross symbols mark the high surge current events. Right: the 500 MHz waveform is collected for the third high surge current event in the left plot.

necessary to provide precise 24 bit pressure and temperature values, which are needed to compensate the pressure measurement. The pressure resolution spans from 0.012 to 0.065 mbar according to different operating modes. The sensor working ranges are 10–1200 mbar and −40–85 °C.

The reading and the calibration compensation of the pressure and temperature sensors, which are non time critical tasks, are directly controlled by the microprocessor, without the intervention of the FPGA.

4. HVPSS performance in a test beam exercise

A fully assembled system has been employed during a test beam exercise in October 2018 at CERN SPS H4 beam line. The system has been operated for nearly two weeks powering one of the electrodes, in particular the MicroMegas mesh of the last multiplication stage of a hybrid mini-pad prototype for single photon detection [7]. During the two week operation, the system has recorded the current provided to the micromesh at the sampling rate of 156 Hz and has recorded several discharge events storing the full waveform at 500 MHz sampling rate. The HVPSS monitoring capabilities are illustrated in Fig. 23, where the measured current versus time is plotted. The data points in the plot correspond to the mean value of the histogram generated in the FPGA block using the decimated data. Each peak in the figure is correlated to the beam extraction, during which the electron multiplication processes occurs in the MPGD and, therefore, the power supply system must provide current to preserve the correct electrode voltage. During the measurement period, the detector experienced different beam setting condition and detector working parameters and these variable conditions can be clearly identified in the current plot, as detailed in the figure caption. Fig. 24 presents a zoomed view of a portion of Fig. 23: the beam duty cycle change as well as the beam intensity change are clearly visible.

High surge current events were detected applying a threshold to the current slope, defined by the variation of the measured current in two consecutive samples collected at 500 MHz. The absolute time stamp of the event is generated when the high surge condition is detected. The timestamp of the event is saved as well as the memory of the FIFO that stores the 32k data samples. The whole information package is provided to the processor, where it is prepared for data transmission to the remote control PC via the TCP/IP protocol.

Fig. 25 provides an example of the standard information from the HVPSS that can both be visualized online via the dedicated GUI and is also saved for offline analysis. The current versus time is shown in Fig. 25, left: the black dots represents the measurements, while the red line is an interpolation between consecutive measurements. The time between the measurements depends on the chosen decimation factor. The cross symbols mark events tagged as discharges. No corresponding spike is visible, as only the average values are available. In Fig. 25 right, the 500 MHz waveform collected for the third discharge event is displayed. The time interval for the waveform collection are defined by the parameters Sample Before Event (SBE) and Sample After Event (SAE) that limit the time range around the event time. Their value can be changed providing high flexibility in selecting the time interval of interest.

5. Outlook

A new version of the HVPSS system prototype is being designed and built. It implements the possibility to remotely modify the picoammeter gain and range by replacing some passive components with electronic controlled ones.

A Fast optocoupled HV switch[16] with insulation capabilities up to 10 kV, directly managed via the FPGA system, will be included in the next picoammeter board revision. It will be so possible to cut, when needed, the HV connection between the detector and the power supply system, therefore limiting the discharge power. The possibility to extend the current monitoring performance achieved also to the voltage monitoring is under investigation.

It is foreseen the connection between multiple single channel setups to create a multichannel system. New logical blocks will be designed to control all the novel features. A communication and broadcast network based on time division multiplexing (TDM) will be implemented. This network can allow local reconfiguration among different setups and the application of feedback protocols to multiple electrodes. External hardware will be designed to ensure high voltage isolation among the different modules. It is planned to use HV digital isolators allowing to send data using LVDS standard at speeds up to 100 MBPS.

6. Summary

The principle of the original HV system denominated HVPSS is presented. A single channel high voltage system matching the needs for the development, study and monitoring of detectors by MPGD technology has been designed and realized, including its hardware and software components. It offers high resolution diagnostic facilities and intelligent dynamic voltage control for detector stability. Both commercial and custom components have been employed for its realization. The commercial components have been characterized and their performance studied in order to select among available devices. Digital design blocks to manage the data acquisition of the high performance ADC has been successfully implemented in the FPGA. An API running in the processor has been designed and tested successfully for communication with a PC using a dedicated GUI.

Galvanic insulation is obtained via an optical fiber networking interface. This prevents the electronic noise to propagate via the ground network and to safely communicate with the remote monitoring PC.

Discharge tagging with 2 ns time resolution has been achieved. Current resolution can be adjusted according to the sampling rate required and to the dynamic range of the monitoring current from 3.9 pA to 400 nA.

HVPSS has been employed to successfully power and monitor the electrode current of a MPGD-based detector for Cherenkov applications operated in a test beam exercise at CERN in 2018.

An improved HVPSS version is being realized as well as a prototype of a multichannel system.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

CRediT authorship contribution statement

S. Carrato: Resources, Writing - review & editing, Funding acquisition. **C. Chatterjee:** Investigation, Validation. **A. Cicuttin:** Conceptualization, Supervision, Investigation, Writing - original draft. **P. Ciliberti:** Investigation, Validation. **M.L. Crespo:** Conceptualization, Writing - original draft, Supervision, Funding acquisition. **S. Dalla Torre:** Resources, Writing - review & editing, Funding acquisition. **S. Dasgupta:** Validation, Investigation, Visualization. **W. Florian:** Validation. **L. García Ordóñez:** Methodology, Software, Investigation, Writing - original draft. **B. Gobbo:** Methodology, Resources, Software. **M. Gregori:** Validation, Resources. **A. Kosoveu:** Validation, Resources. **S. Levorato:** Project administration, Funding acquisition, Conceptualization, Methodology, Writing - original draft, Visualization, Supervision, Validation, Resources, Investigation. **K. Mannatunga:** Resources, Software. **G. Menon:** Resources. **S.M. Hashemi:** Resources, Investigation. **F. Tessarotto:** Conceptualization, Investigation, Resources, Supervision. **Triloki:** Writing - review & editing. **B. Valinoti:** Resources, Validation, Writing - review & editing. **Y.X. Zhao:** Resources, Investigation, Writing - review & editing.

[16] OC100HGwww.voltagemultipliers.com.

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